Cadence OrCAD and Allegro: What's New in Release 22.1

This document describes the new features and enhancements in Cadence® OrCAD® and Allegro® products in release 22.1.

Allegro PCB Editor and Allegro Package Designer Plus

This section describes the new features and enhancements in Allegro® PCB Editor and Allegro® Package Designer Plus, in release 22.1. If a feature is available in only one of the layout editors or for a specific license, a note is provided.

Migrating to Release 22.1

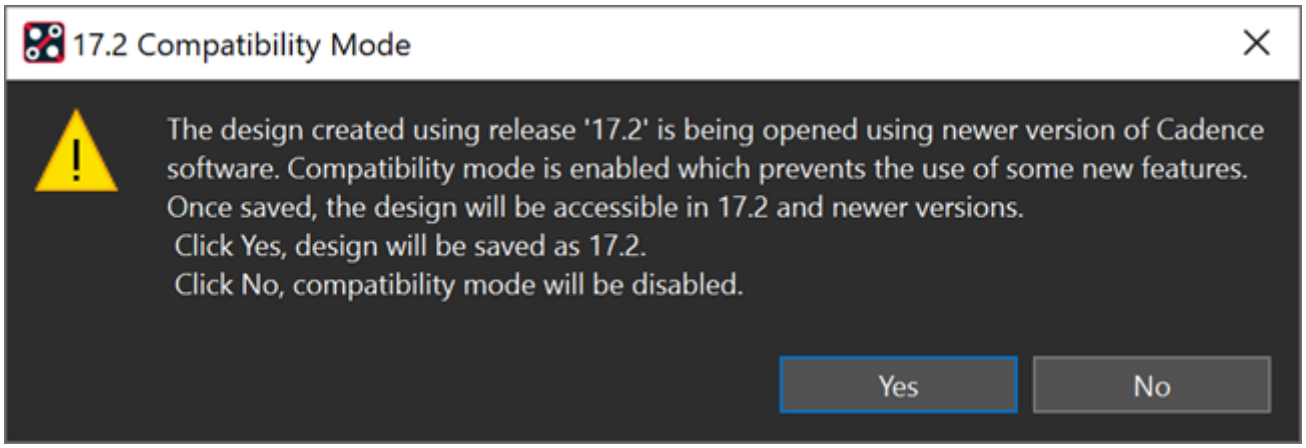
Although the database format has not changed between releases 17.4-2019 and 22.1, you still need to acquire new licenses and an account to work with *Mirrored Layers* as explained in the following sections:

- Database Format
- License Updates
- Structures and Vias in Mirrored Layers

Database Format

You can open any release 17.4-2019 design in release 22.1 or, conversely, a release 22.1 design in release 17.4-2019 without any need to migrate the database format because the same database format is used across the two releases.

The *17.2 Database Compatibility Mode* can still be enabled in User Preferences Editor to allow release 17.2 designs to be opened in releases 17.4 or 22.1 without updating the database version. Designs opened in the compatibility mode can be opened in release 17.2.



Important

The new features of release 22.1 or 17.4-2019 are not available in the database compatibility mode. To use the new features, deactivate the database compatibility mode. To revise the database to be opened in release 17.2, run the downrev process.

License Updates

A new license file is required to run release 22.1 products. Products from earlier releases such as 17.x, can also be opened with a release 22.1 license.

Structures and Vias in Mirrored Layers

If a database has structures in the *mirrored layers* state, that is marked as `mirrored_layers`, the database cannot be migrated to a version earlier than release 17.4 -2019, HotFix 028 (QIR4).

The objects in the mirrored layers state are structures that are flipped using the *Mirror Geometry* command and then mirrored to the opposite side of the board.

It is common to use the *Mirror Geometry* command to flip a structure on the same layer, but vias can also be flipped when moved or copied and if such vias are part of a symbol, module, or group, mirroring changes the vias to the Mirrored Layers state.

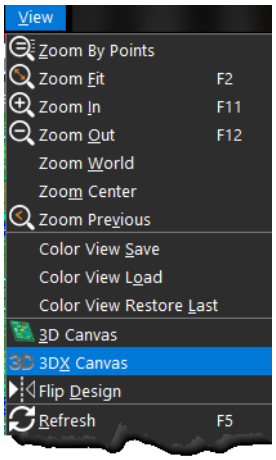
See *Migration Guide for Allegro Platform Products* for details on how to identify, locate, and update Mirrored Layer objects when you downrev to an earlier version that does not support Mirrored Layers.

Memory Usage and Performance Improvement Using 3DX Canvas

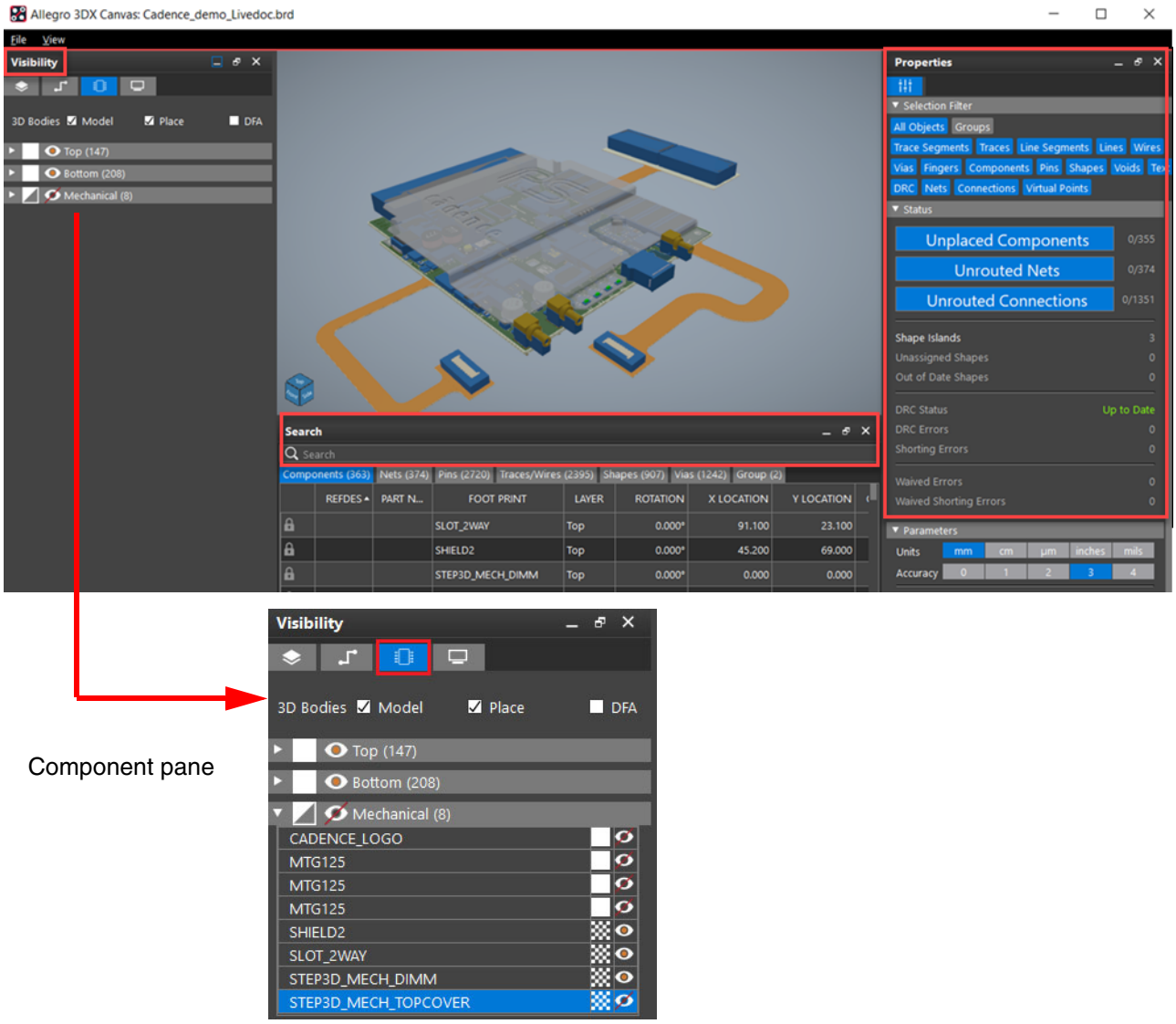
Note: The 3DX features are only available with the *Allegro X* licenses.

This release comes with a new 3DX engine which is integrated with the Allegro board design database to address the scale and complexity issues related to large designs involving performance and memory usage in the erstwhile 3D canvas. 3DX Canvas provides quicker and more efficient handling of large designs.

The 3DX Canvas window can be accessed from the *View – 3DX Canvas* menu command or the *3DX* toolbar icon:

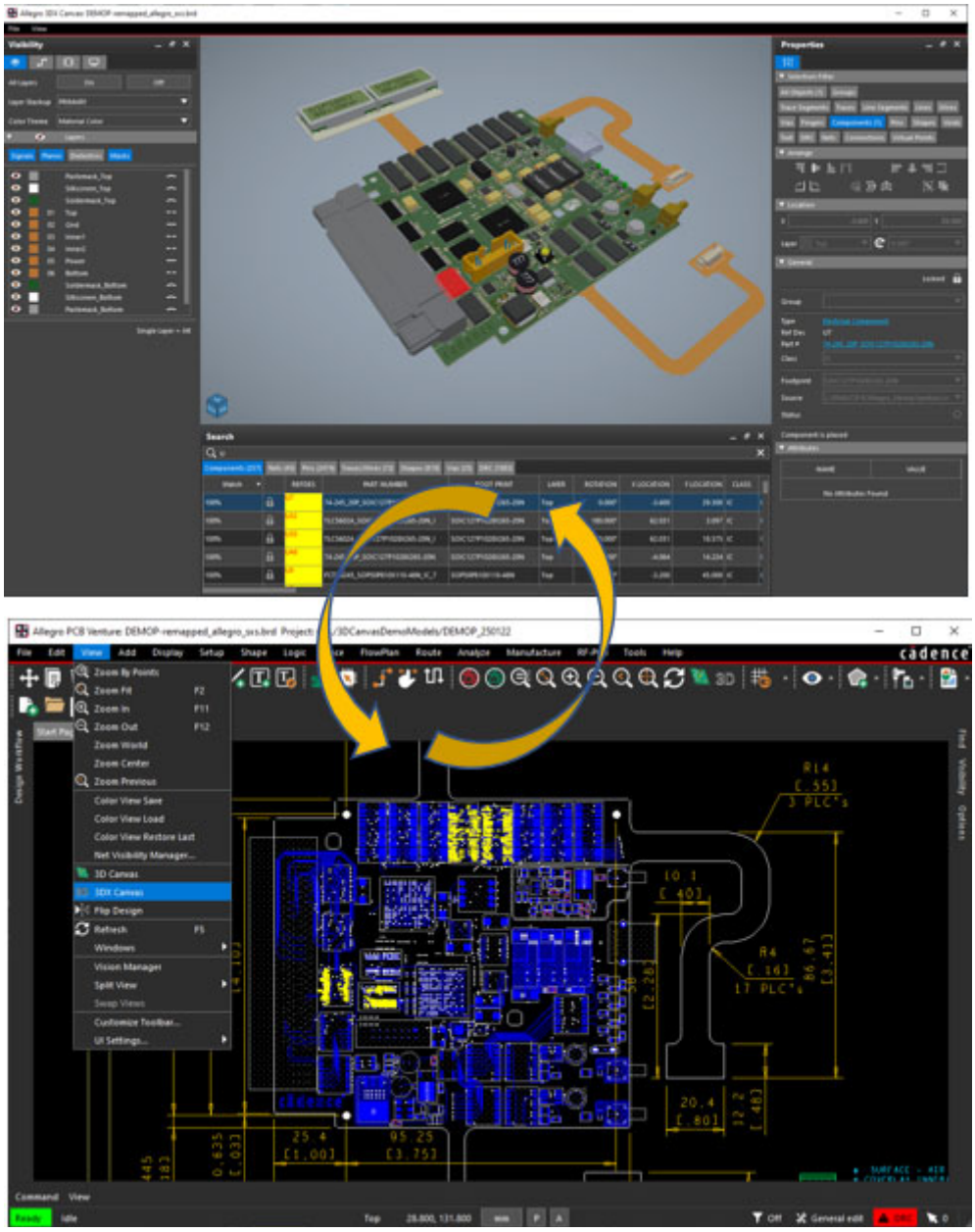


The 3DX Canvas window includes the *Visibility*, *Properties*, and *Search* panels and the *Component* pane.



Component pane

The 3DX Canvas view is in sync with all the changes made to the Allegro database. Any changes made in the layout propagate to 3DX Canvas and the objects selected in the 3DX Canvas window are also selected in the 2D layout, simultaneously.



Although a majority of design changes result in incremental updates to the 3DX view, certain global changes, such as board outline or stack-up changes, might result in reloading of the 3DX view.

For more information about Allegro 3DX Canvas, refer to *Allegro 3DX Canvas User Guide*.

High-Speed Structure Enhancements

High-speed structures have been improved to speed up creation. Now you can also create structures that do not contain pad entry or exit traces maintaining current routing and delayed matching. Structures can also be redefined to overwrite an existing structure or to create a new structure.

The following sections describe the structure enhancements:

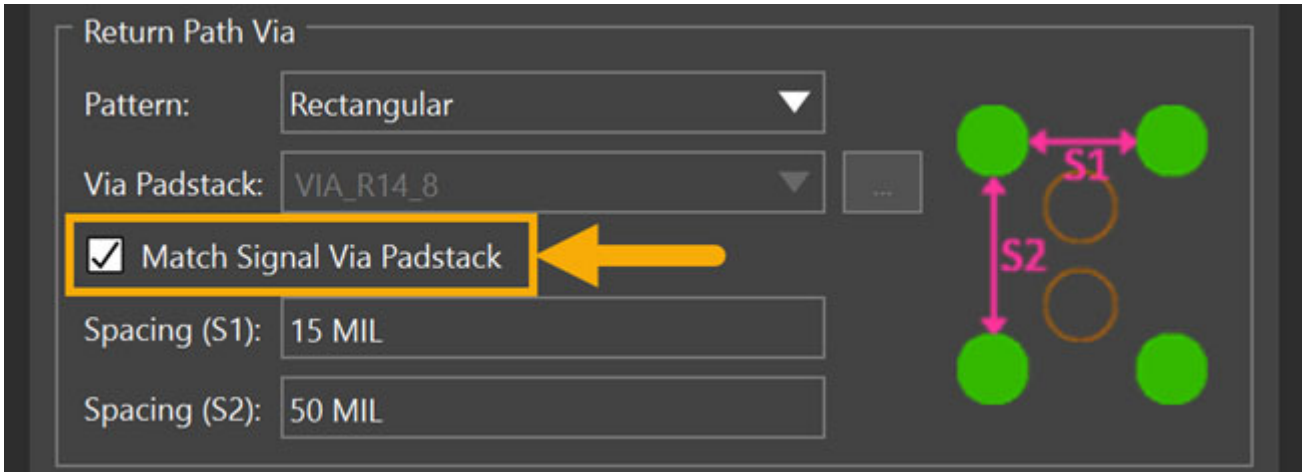
- Parameterized High-Speed Structures
- Differential Pair Vias Replaced by Structures
- On-Canvas Structure Update and Variant Creation

Parameterized High-Speed Structures

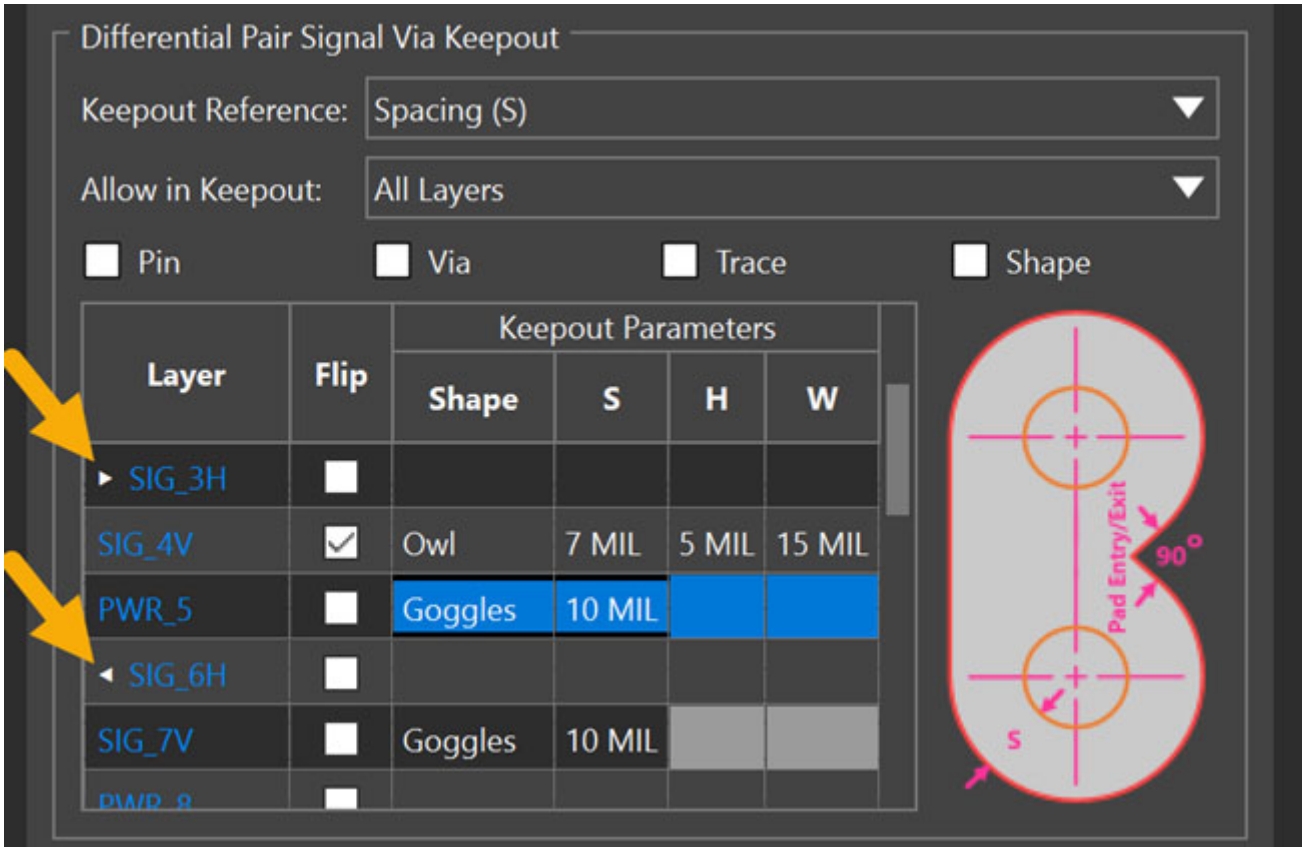
Note: Parameterized high-speed structures are only available in the *Allegro PCB Designer* product with the *High-Speed* option.

Creating structures is now faster because information from other areas of the form is leveraged. This information is extracted from the Differential Pair transitions selected on the canvas. This is an enhancement over the prototype introduced in release 17.4-2019, HotFix 013 to generate structures based on parameters.

- The Return Path vias use the same padstack as the signal transition vias. To leverage this fact, a new option to match the Signal Via transition padstack is now available:



- Differential Pair Via transitions require adjacent layer keepouts. When defining keepouts, the location of pad entry or exit traces must be known. Layer rows now have a directional triangle to identify that pad entry or exit traces are present.

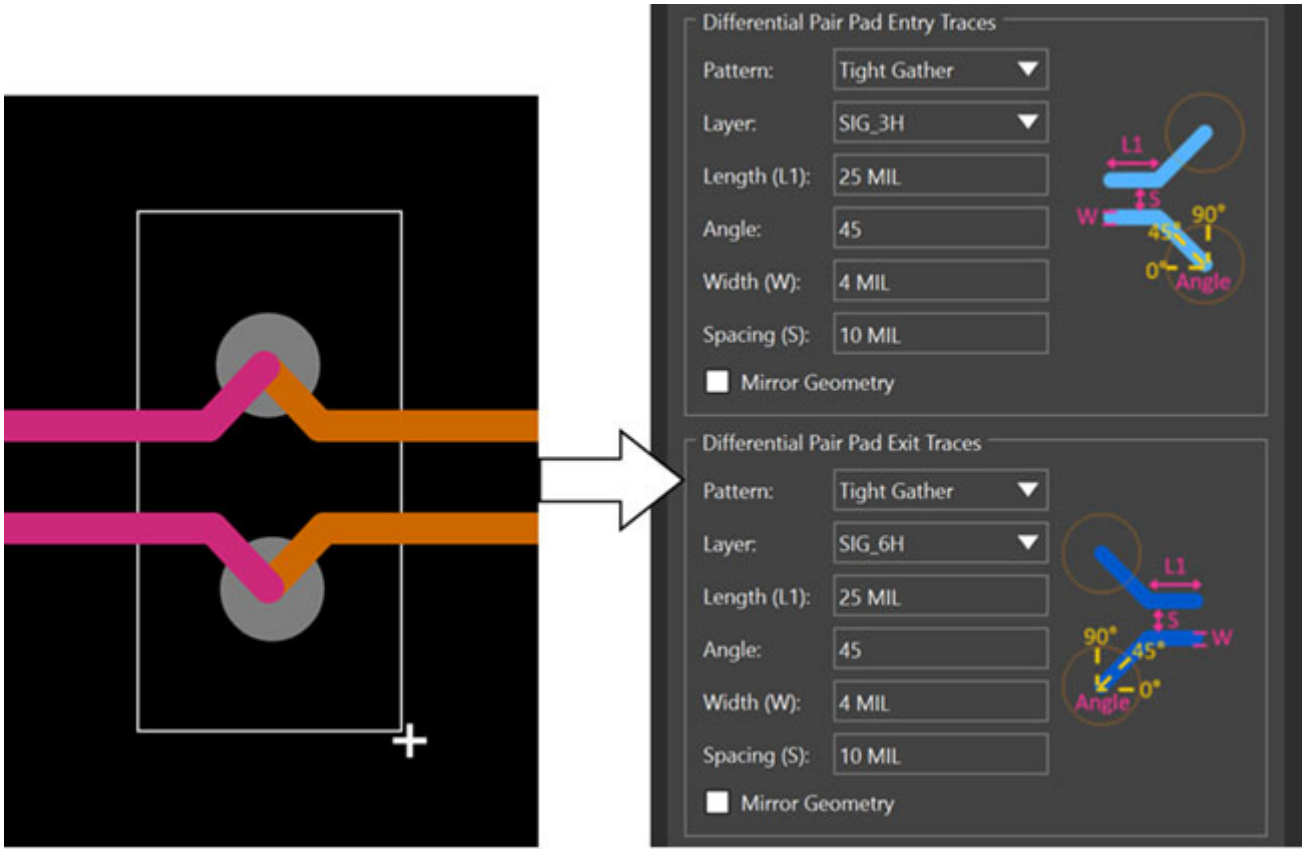


- Differential Pair routing can be completed prior to receiving Return Path Vias and Adjacent Keepouts requirements from Signal Integrity. Leveraging Differential Pair Via

transition information from the canvas makes it easier to create a compatible structure for replacement.

- Selecting an existing Differential Pair via extracts the signal via padstack as well as the pad entry or exit trace information:
  - Trace Pattern detection – Tight Gather, Loose Gather, and Tandem
  - Current Trace Layer, Width, and Spacing

- Mirror setting when pad entry or exit traces are on the same side:



Differential Pair Vias Replaced by Structures

Note: This feature is only available in the *Allegro PCB Designer* product with the *High-Speed* option.

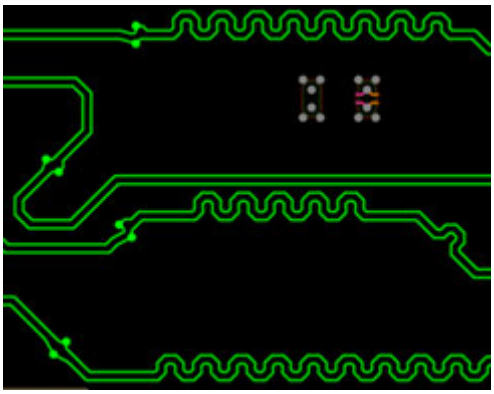
In this release, the *Replace Via with Structure* option is updated to accept structures that do not contain pad entry or exit traces maintaining current routing and delay matching. The ability to quickly replace Differential Pair vias with structures was provided in release 17.4-2019, HotFix 028. Although this automatic replacement works well, if pad entry or exit traces

are adjusted to meet timing requirements, the replacement can cause delay DRCs that did not exist before the replacement.

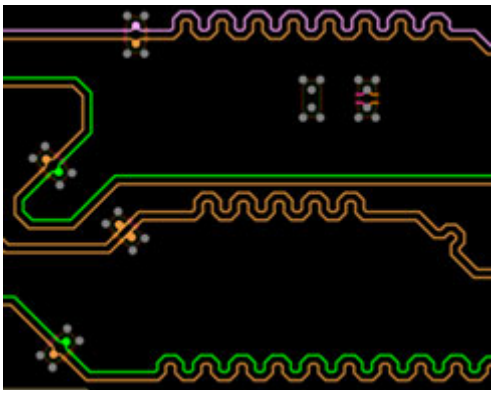
Using the Replace Via with Structure option...

Display in Timing Vision...

Matched routes display in green in Timing Vision.



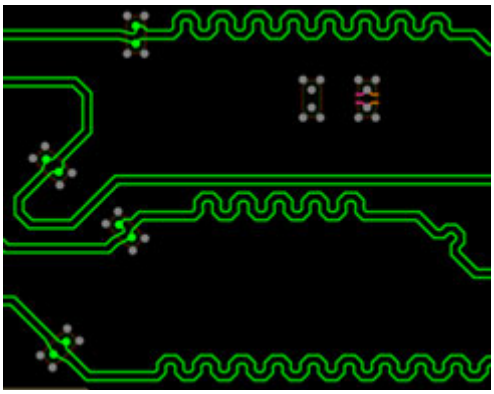
Replacing via with Structure containing pad entry and exit traces maintains connectivity, but reports a matching failure in Timing Vision.



Using the Replace Via with Structure option...

Structure with Return Path only reports green in Timing Vision and Pad Entry and Exit are maintained.

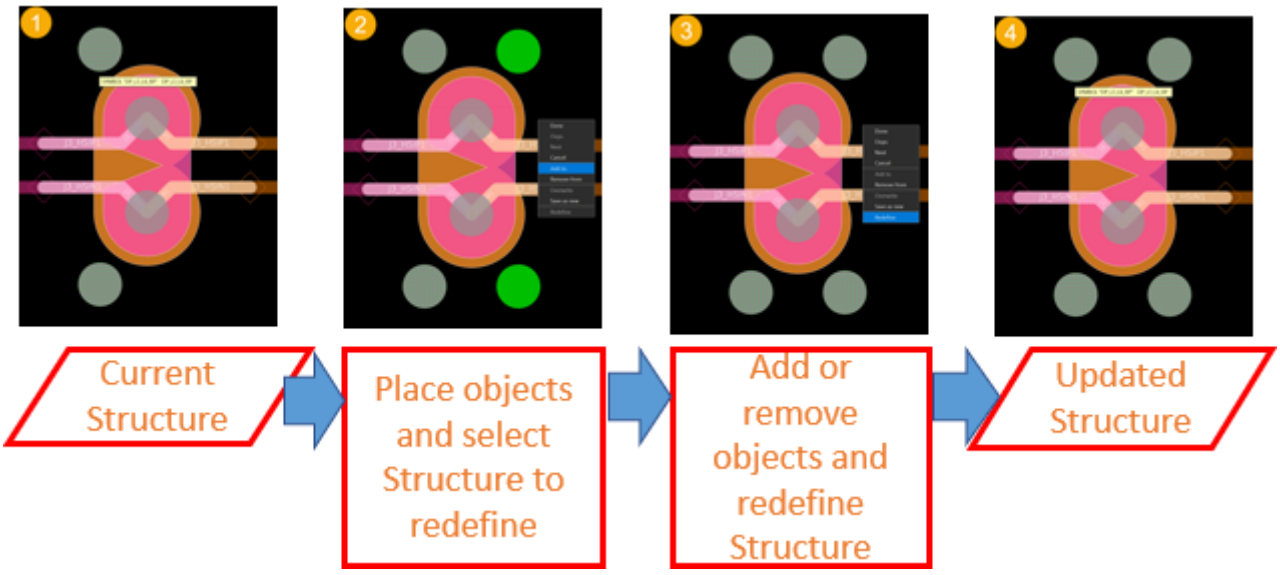
Display in Timing Vision...



On-Canvas Structure Update and Variant Creation

Structures can be used multiple times in a design. One instance can be updated and the changes can be pushed to all the other instances. At times, you might need to add or remove objects, or create a slightly different variant of a structure for different applications. In this release, the *Route – Structure – Redefine* command is introduced to add or remove objects from an existing structure. You can then overwrite the instances or save to a new structure, using a shortcut command.

The existing flow of moving or adjusting structure objects, without changing membership, can still be used by selecting a structure using the *Redefine Structure* command to push updates to all the instances.



Note: To access the new command *Redefine Structure*, you must add the following in the `PCBENV/ENV` file:

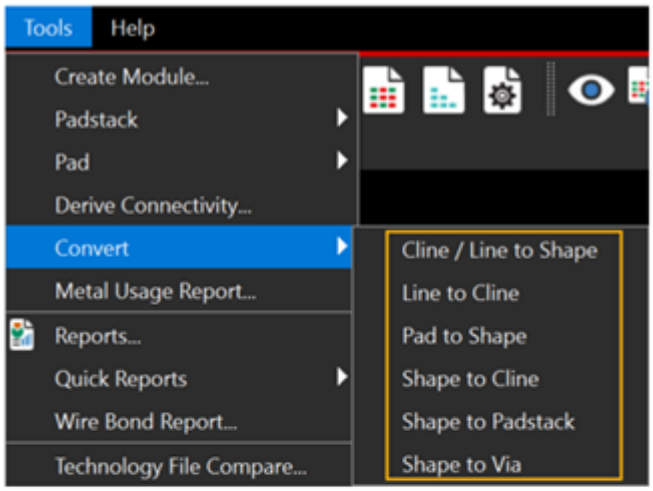
```
set VIA_STRUCT_REDEFINE_CANVAS
```

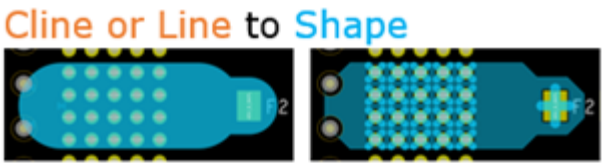
Converting Shapes, Vias, and Pins

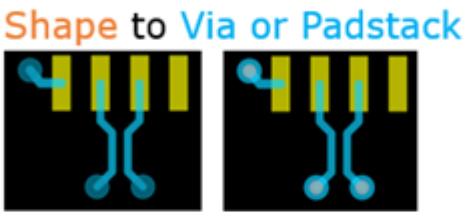
Note: This feature is only available in the *Allegro PCB Designer*, *Allegro X Designer*, *Allegro X Venture Layout*, and *Allegro Package Designer Plus* products.

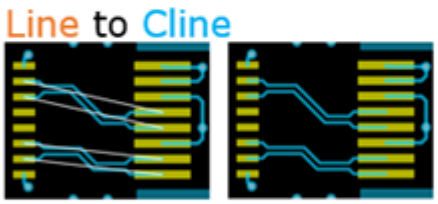
Converting the `GERBER` or `DFX` files into intelligent designs sometimes requires conversion of these files to a different design object to establish connectivity. For example, some import results in Shape objects where Vias and Pin objects are required or Line objects where Cline (connect lines) objects are required. Another design activity is generating custom Shapes based on Clines, Lines, and Pin or Via Pads instead of tracing objects manually.

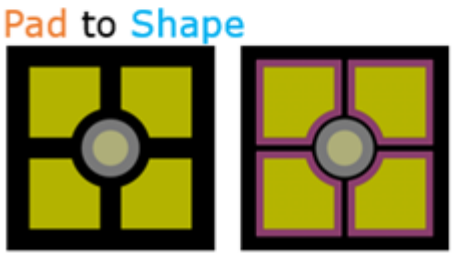
This release introduces several utilities to convert objects and create or replace an object with a padstack directly on the canvas using the commands under *Tools – Convert*.







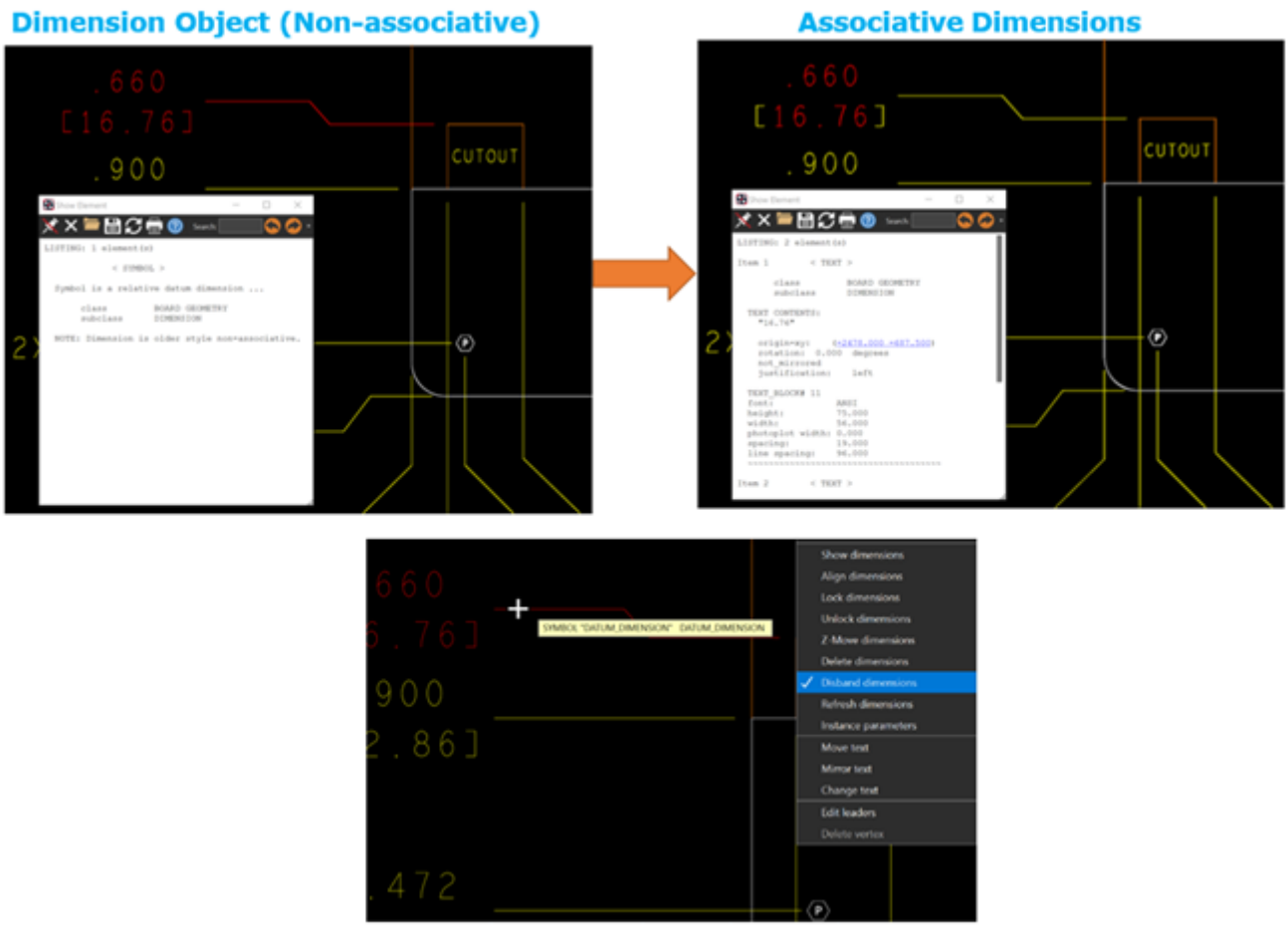




Dimensioning Update

The *Dimension Environment* command provides the ability to create associative dimensions between objects in the design. As a result, when a dimensioned object is moved or changed, the dimension is updated automatically. Although automatic update of dimension is useful, switching to Dimension Environment to delete or modify a dimension can be a tedious task. Also, non-associative dimensions are locked and can only be deleted and regenerated. Even minor re-adjustments to a dimension require the tedious task of deleting and regenerating a dimension.

In this release, you can separate dimension symbols into individual objects to make changes to a dimension without deleting and regenerating it. To separate a dimension into individual unassociated objects, choose *Manufacture – Dimension Environment,* and then choose the *Disband dimensions* command. This command can be used on both the legacy (non-associative) as well as associative dimensions.



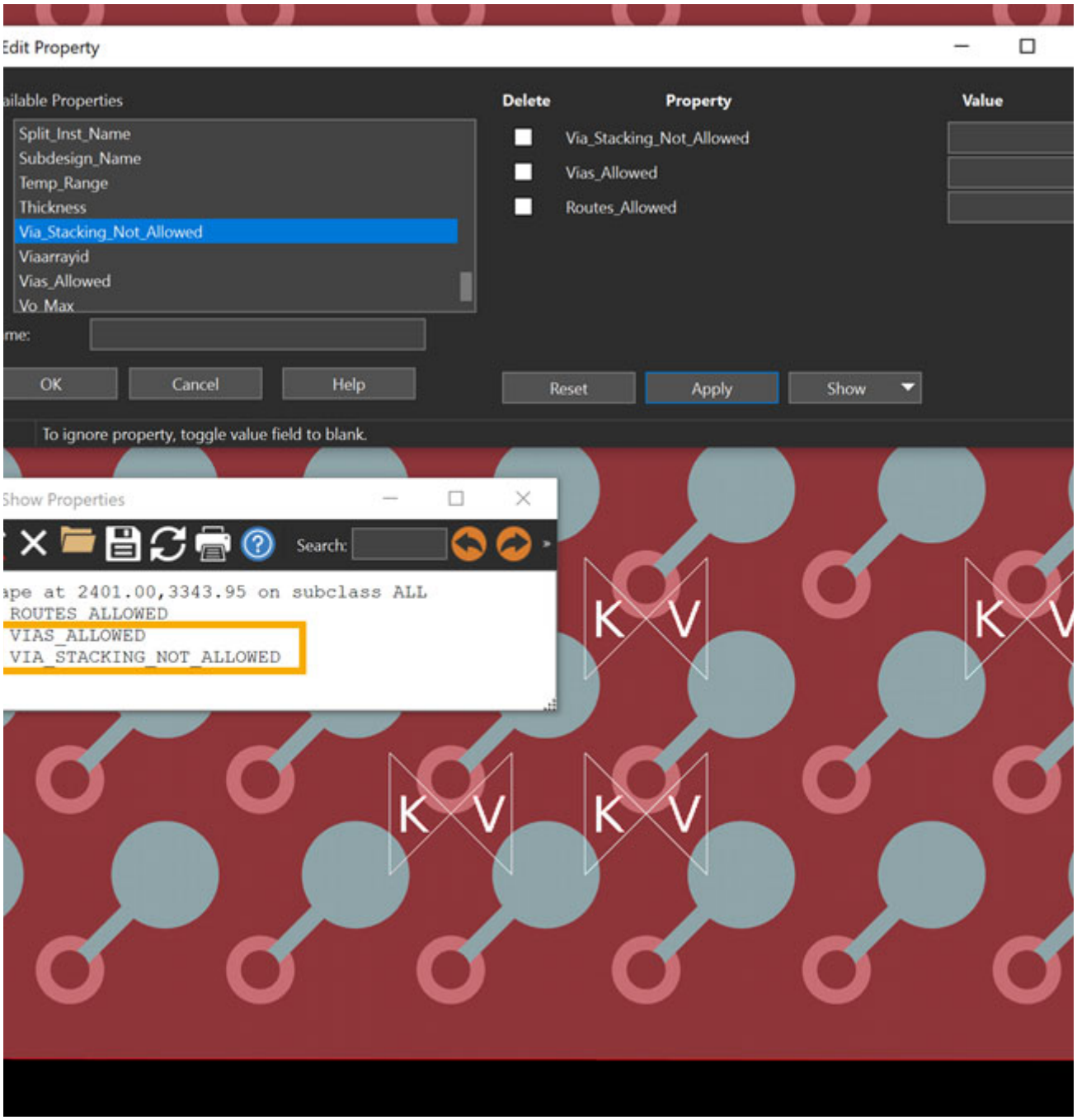
Manufacture - Dimension Environment - Disband dimensions

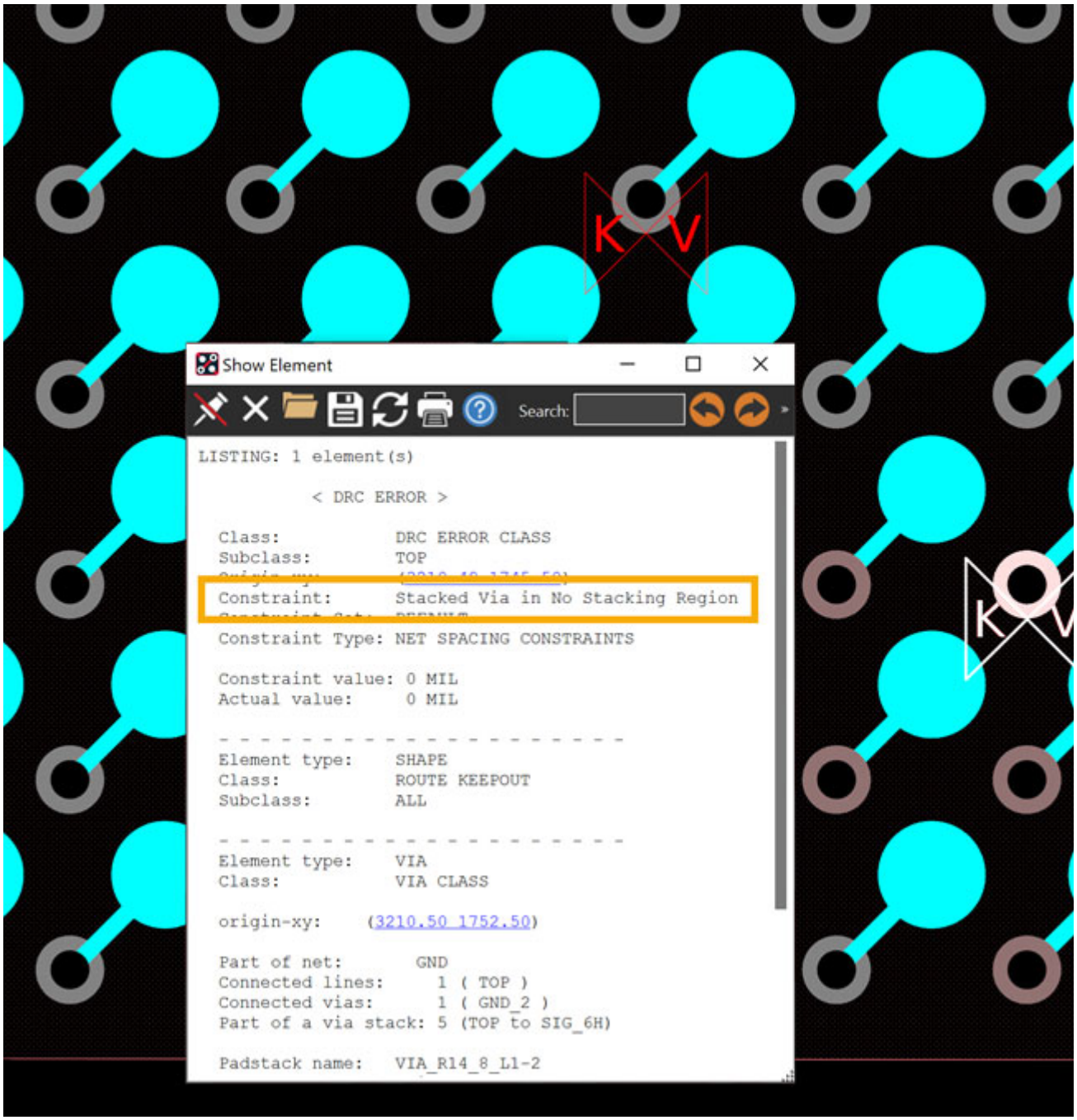
Route Keepouts Exception Use Model Enhancement

Although stacked vias are common in designs today, they cannot be used in some areas of the designs. You can, of course, use constraint regions with a via list check but that can lead to other complications with false DRC Errors.

The enhanced exception use model for the Route Keepout shapes with a new Shape property called `VIA_STACKING_NOT_ALLOWED` provides a simple method to detect where stacked vias are located and flag DRCs in restricted areas. Attach this property, along with `VIAS_`

ALLOWED to a Route Keepout shape so that vias can be added inside the keepout but DRCs get displayed when stacked vias are present.





Performance Enhancements

Enhancements have been made in release 22.1 to speed up design time. Some of the major performance improvements in this release are as follows:

Better Performance in Designs with Large Number of DRCs

Designs that have a large number of DRCs are now faster. For example, deleting DRCs is faster by up to 450 times for commands that needs to query or delete DRCs. Tasks that result in changes in the DRCs, such as adding or moving objects in bulk or shape updates, are also faster.

Faster Update to Smooth

The *Update to Smooth* command is now significantly faster because of a new PolyBool engine and improvements in Shape Trim work. For example, in certain instances, the time required to run the *Update to Smooth* command has reduced from an hour to about 2 minutes.

Better Move Performance

Moving large modules or big complex structures is now faster. For example, the time needed to move large modules has reduced by up to 19 times, taking 5 seconds instead of the earlier 82 seconds. Similarly, moving a complex structure that took 18 minutes, now takes only 1.2 minutes.

Better Performance for Shape Parameter per Layer Override

When overrides inside of the *Dynamic Shape Layer Parameters* dialog box are used, the performance has improved for various commands, such as *Add Connect*, *Slide*, *Move*, and *Structure Redefine*.

Restricting Command Window Messages

Non-critical messages for design tasks are no longer visible in the Command window. For example, often while performing large operations, more than 1000 messages were displayed earlier. The maximum number of messages is now restricted to 100.

Faster DRC Checking on Designs with Negative Layers

DRC performance on designs with negative layers has improved in this release. For example, Negative Island check is now 20 times faster.

Display Enhancements

In this release, the display is enhanced to ease the design process for complex and dense designs. The following sections describe the display enhancements:

- Expanded GPU Support
- Normalized Forms for High Resolution Displays

Expanded GPU Support

Note: This feature is only available for the *Allegro X Venture Layout* product.

In this release, in addition to the existing support for NVIDIA GPUs, the GPU Canvas rendering is expanded to support modern discrete or integrated GPUs from Intel and AMD with the following enhancements:

- Performance gain in panning and zooming
- Augmented quality of display:

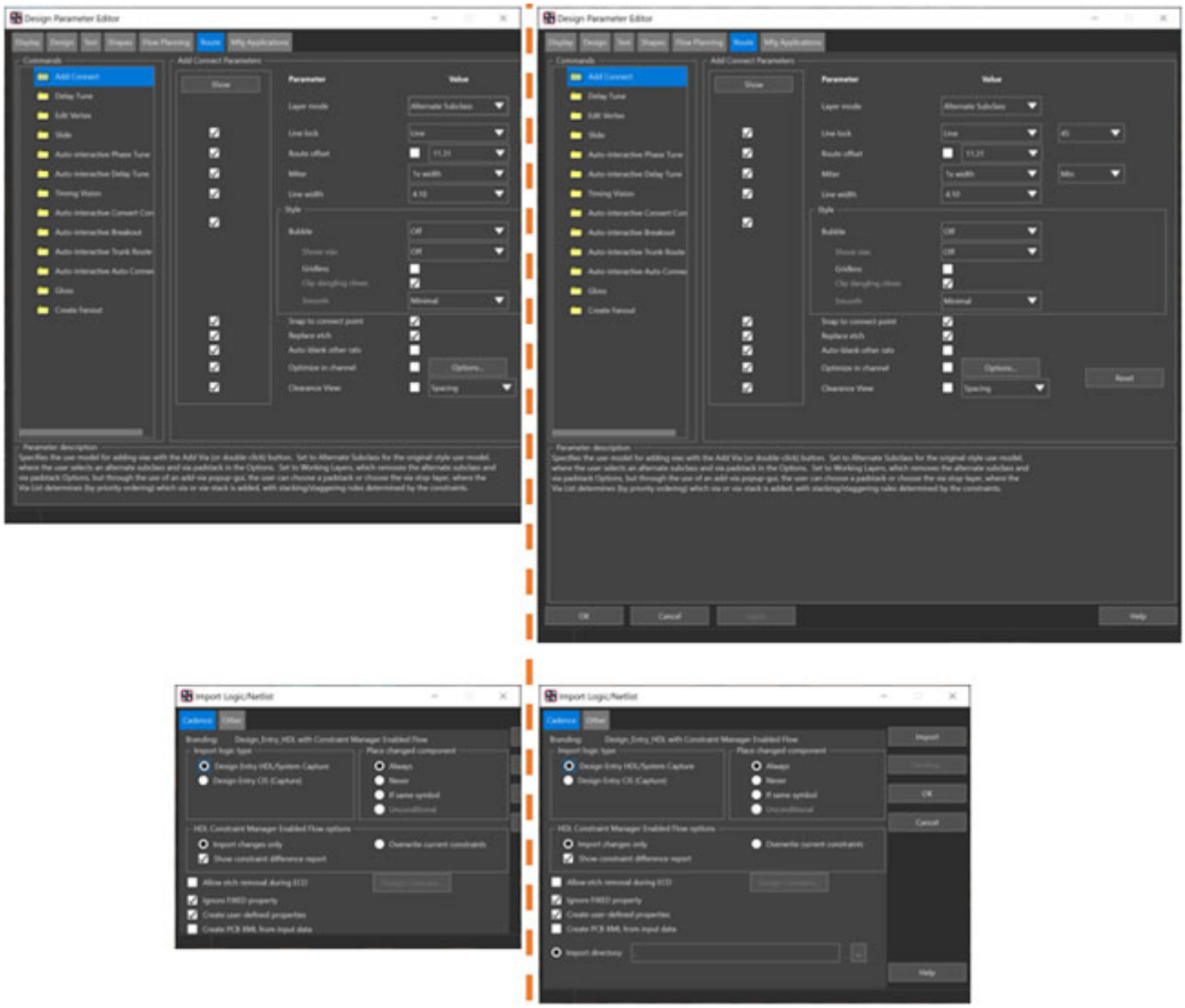
  Virtual machines require a dedicated or integrated NVIDIA, Intel, or AMD physical GPU.
- The best possible GPU renderer is detected and enabled automatically when starting layout editors:
  - To disable GPU Canvas set the `DISABLE_GPU` variable in the *User Preferences* setting.
  - To disable GPU Canvas for a session use the`-nogpu` switch (`allegro -nogpu`).

Note: This is a prototype feature for early adopters. You must enable the following environment variable to load a plugin to try out the new GPU Canvas:
`set PG_PLUGIN_PATH $ALLEGRO_INSTALL_ROOT/tools/plugins/gpu`.

Normalized Forms for High Resolution Displays

You can now specify a scaling factor to normalize forms that are partially cut off due to display scaling. High-resolution display devices with 4K or higher resolution use display scaling to improve display visibility. However, some sections of forms are truncated due to scaling.

In this release, use the system variable `ALLEGRO_HIGH_DPI_ENABLED=1` to accept a scaling factor number (`1.25`) to normalize form content. The images on the right are scaled by a factor of `1.25`



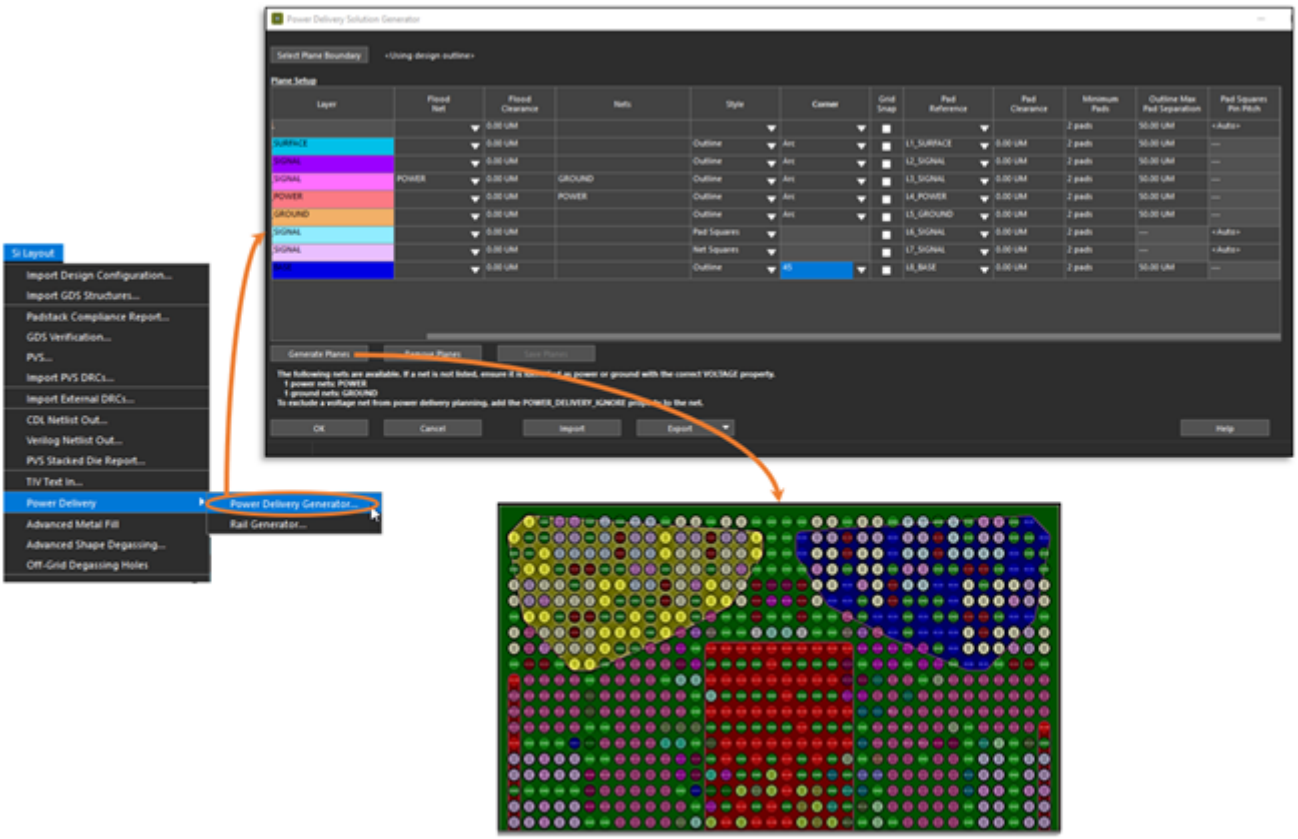
Power Delivery Generator

Note: This feature is only available for the *Allegro Package Designer Plus* product with the *Silicon Layout* option.

With Power Delivery Generator, there is no need to define the plane areas manually by highlighting power nets in the layout and then looking for clusters. You can now build plane

areas based on the location of the pins in the layout that reference the planes and the application takes care of the rest.

The Power Delivery Plane Generator (*Si Layout – Power Delivery – Power Delivery Generator*) function creates Power and Ground planes based on the locations of pins or vias within the target area.



Outline - Region defined by a bounding shape, convex_hull

The plane boundary can range from a flood net to cover the layer where no other plane is poured, to regions defined by a bounding shape (convex hull) surrounding pin groups, to rectangular regions such as blocks around regular clusters of pins that identify power domains inside of the chip.

Note: You can only select the power and ground nets with Ratsnest Schedule and Voltage properties.

You can continue to change parameters as the design progresses and regenerate all the planes as and when needed.

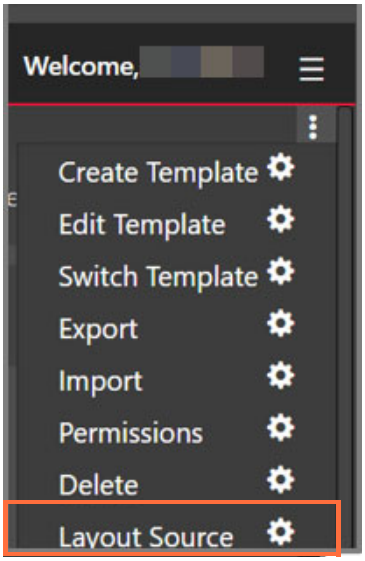
Allegro Pulse and Allegro EDM

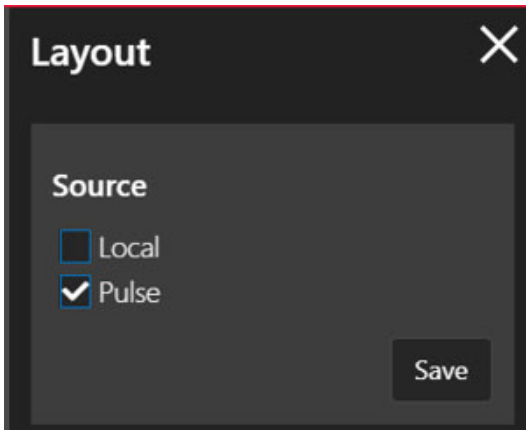
This section describes the following new feature in Allegro® Pulse and Allegro® Engineering Data Management (EDM) in release 22.1.

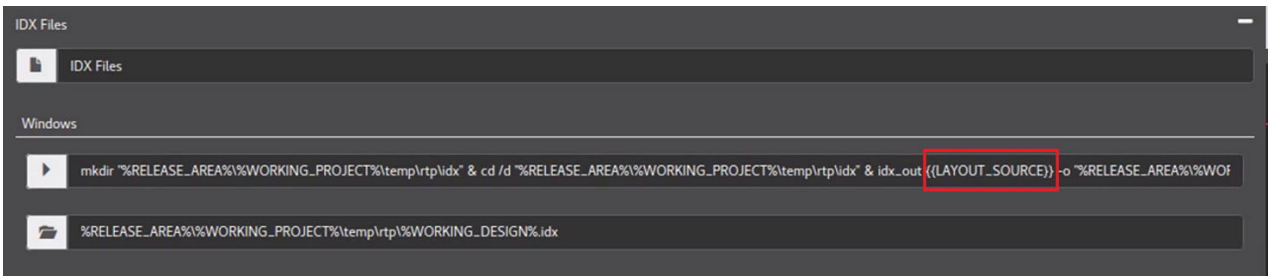
Pulse as a Layout Source

If you work with boards outside of Allegro System Capture, you can define a single source for a layout design in the Administration mode of the Publish for Manufacturing (PFM) application. You can then specify this layout source in the PFM utilities to locate the layout design in a simplified, consistent manner.

In addition to a local source such as `<proj>/output/<design>/physical`, you can now use Pulse as the layout source. Within the PFM utilities, the variable `{{LAYOUT_SOURCE}}` can then be used to locate the layout design.



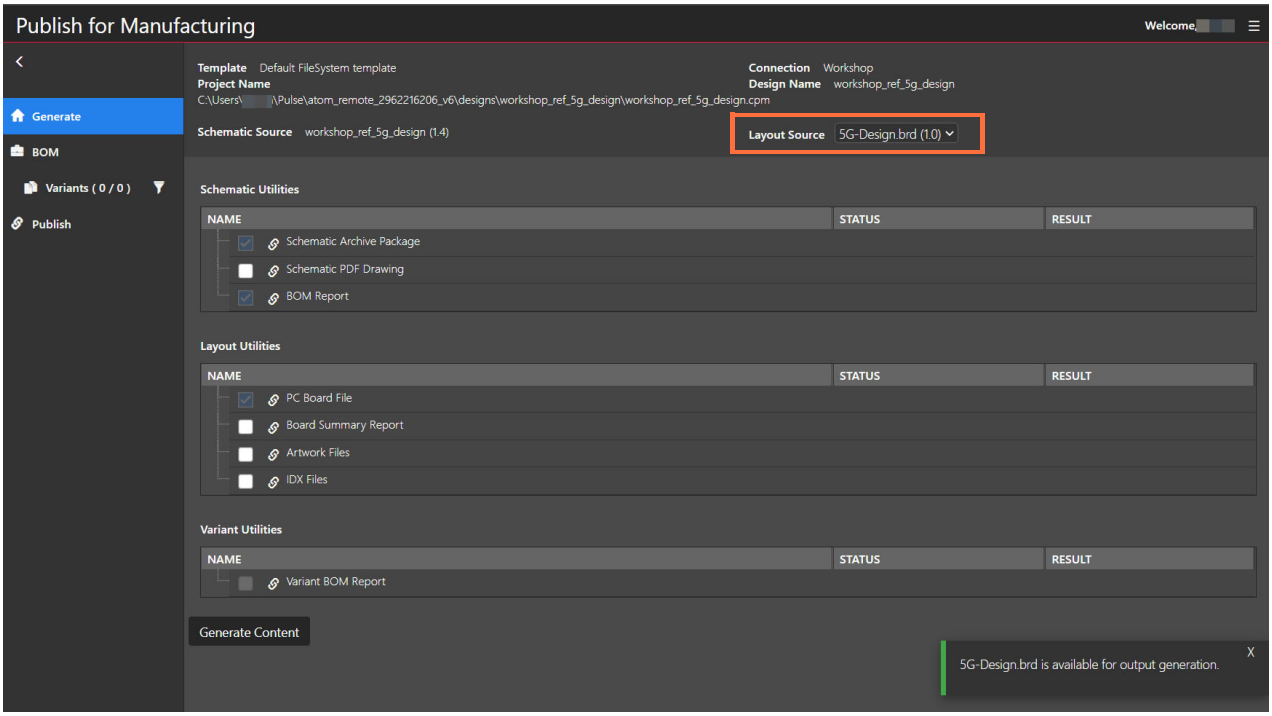




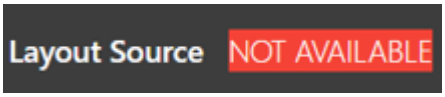
In Pulse, you can maintain a link between the schematic design version which generated the netlist for the layout, and the layout version from which changes were backannotated to the schematic. For details, refer to *Linking Schematic and Layout Versions* in *Allegro System Capture Pulse User Guide*.

When Pulse is specified as the layout source, you can also select the layout from which derived content is to be published to the PLM system. When a designer launches PFM with

a publish template that uses Pulse as a layout source, the latest committed version of the layout is downloaded to a project subfolder (`temp/layouts`). All utilities specifying the `{{LAYOUT_SOURCE}}` variable use this layout design when generating outputs.



If Pulse is selected as the *Layout Source* without any linked layout for a design, PFM displays the following status:



For details on specifying Pulse as the layout source, refer to *Publish for Manufacturing User Guide*.

Allegro System Capture

This section describes the following enhancements and new features in Allegro® System Capture in release 22.1.

Schematic Accelerators

This section describes the new and enhanced features that you can use to enhance your productivity when working on schematic designs.

Performance Enhancements

In this release, changes have been made to improve the performance and response times for many aspects of schematic designing, including the following:

- Opening and saving designs

  System Capture design and library data on disk now uses industry-standard compression-decompression methods. This has resulted in 2x to 5x improvement in project open, save, archive and other related disk IO operations.

- Wiring performance

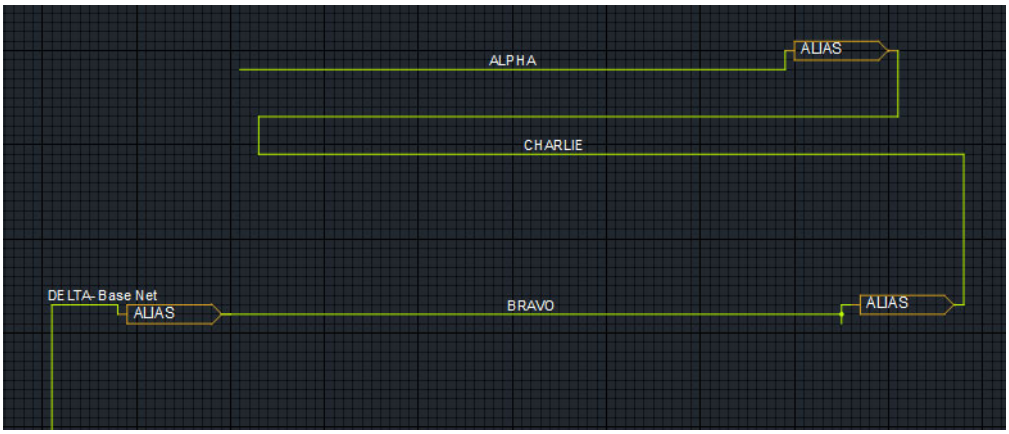
  The interactive wiring performance has been improved by 2x to 5x with a new real-time algorithm for junction calculation and improved data caching.

- Canvas selection

  Selection performance has also been improved by 3x to 5x for large schematic selections.

Displaying Base Net Indicators

When multiple nets are aliased, the winning net name is used as the physical name. You can now configure System Capture to show the winning or base net on the canvas. For example, in the following image, the net `DELTA` is the base net. The suffix you see next to the net name is called a text overlay and can be customized.



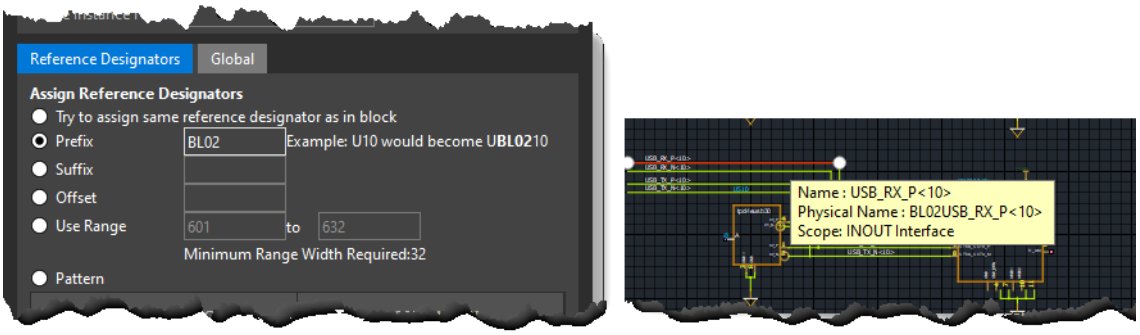
To configure this behavior, set the following directives in the `CANVAS` section of the `site` or *`project`* cpm file:

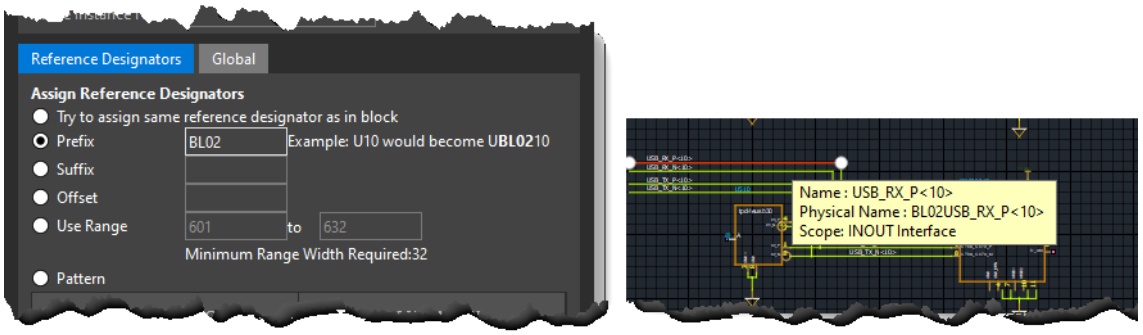
Directive	Value	Description
`BASE_NET_OVERLAY`	`ON`	Enables the feature
`EXPLICIT_BASE_NET_IDENTIFIER`	*`<text>`*	The text to be shown as the suffix for the base net. In the example, this is set to `' - Base Net'`

Prefix and Suffix Extended to Physical Net Names

When blocks are placed in hierarchical designs, you have the option to specify a prefix or suffix for the block. This prefix or suffix is now also applied to the physical net names for nets

or buses. No additional setup is required for this feature. The following images show the effect of setting prefix and suffix on the physical names of nets, respectively.



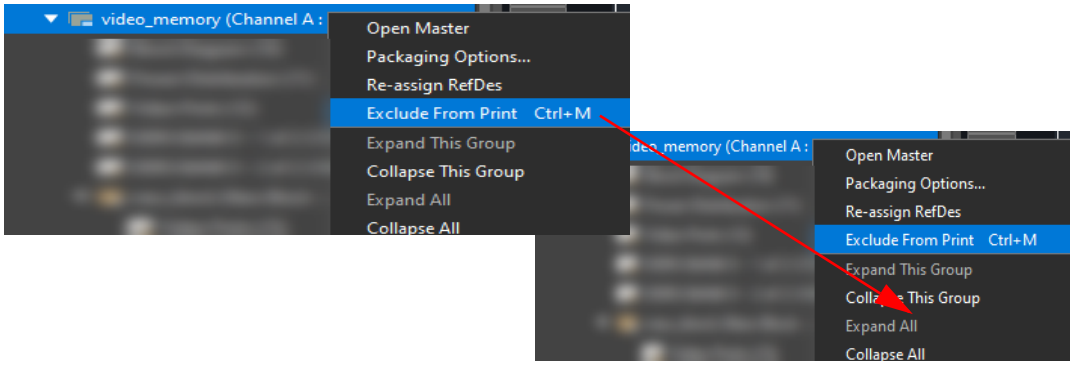


Block Printing Support

By default all the blocks and pages in a design are printed. To restrict the printing of certain blocks, set the `PRINT_EXCLUSION` directive in the `site.cpm` or *`design`* file as

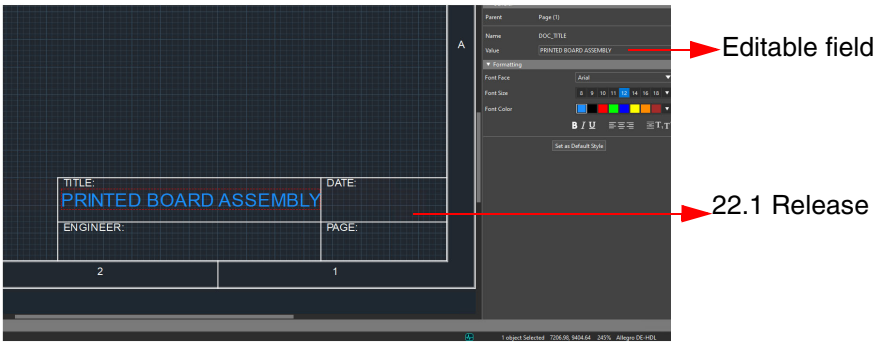
```
PRINT_EXCLUSION 'true'
```

Now, when you right-click a block, a new option *Exclude From Print* is available. When selected, an icon shows that the block will not be printed.



Support for Properties on Page Border

Until now, for the designs migrated from DE-HDL and page border symbols from DE-HDL libraries, properties on page border were being annotated as notes. This has now changed and these properties are now brought in as properties. For the property placeholders defined on the page border symbol, designers can now change the property values too. But not change the visibility. The following image shows the change:



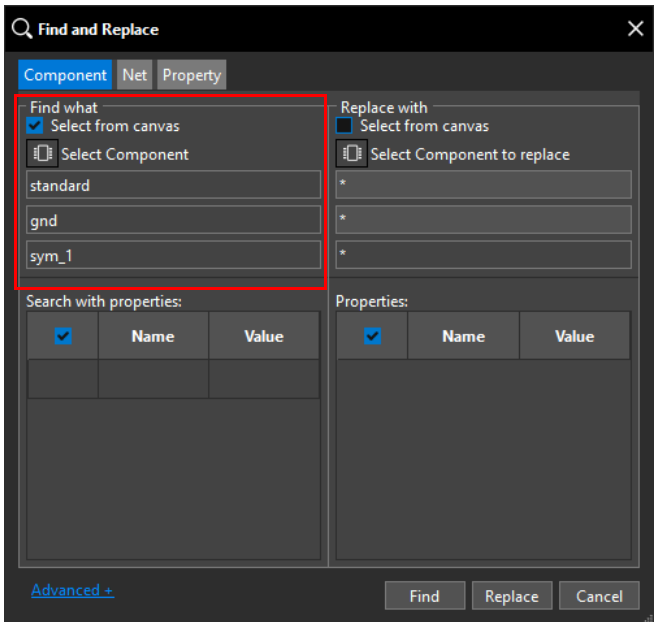
Open Projects as Read-Only

To avoid accidental editing of designs especially in a team design environment and to avoid locking a design block or page, a new control is introduced in this release.

When this option is enabled, designs open with a read-only watermark on the canvas and a note to the top-right showing the read-only status even if some design objects are locked. To enable editing, click *Edit Design*.

Finding and Replacing Special Symbols

The Find and Replace feature is now enhanced and you can replace special symbols, such as power, ground, or ports. The special symbols can be selected on the canvas or picked from the *Universal Search* window that opens when you click *Select Component*.



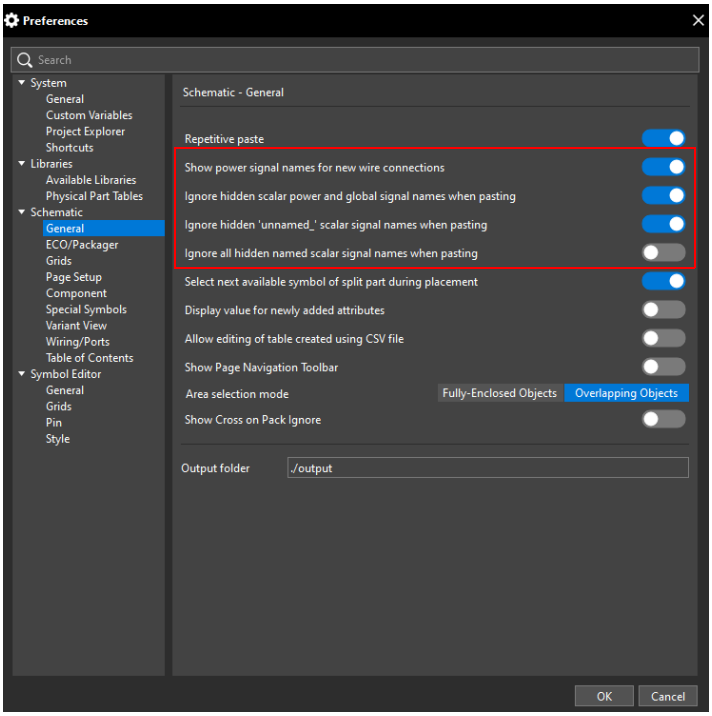
Controlling Signal Name Copy and Assignment

Until now, when connected to a power source, signal and wire names were automatically assigned and displayed. Additionally, when circuitry was copied and pasted, hidden signal names got added. Based on user feedback, the default behavior can now be configured. Directive to control the display of signal names can be added to the `site.cpm` or set in the *Preferences* window.

You can now control the following and benefit from the WYSIWYG display of signal names:

- Adding or displaying the signal name on wires when connected to a power source
- Transferring the hidden power signal name on pasting a selection if the attached power source is not copied along

- Transferring the hidden named and ‘unnamed_*’ signal names when pasting a selection



The corresponding directives for these preferences are as follows:

Directive	Default
SHOW_POWER_SIGNAL_NAMES_FOR_NEW_CONNECTIONS	True
IGNORE_HIDDEN_SCALAR_POWER_SIGNAL_NAMES_WHEN_PASTING	True
IGNORE_HIDDEN_UNNAMED_SCALAR_SIGNAL_NAMES_WHEN_PASTING	True
IGNORE_HIDDEN_SCALAR_SIGNAL_NAMES_WHEN_PASTING	False

Operations that are affected by these controls include:

- Adding a new connections to power sources
- Renaming nets
- Tapping power nets to buses
- Copying circuitry without the attached power sources
- Deleting power signal names from a route island if no power source is attached

Reference Designator Preservation

In earlier releases, the Reference Designator (Ref Des) for multi-section instances or split instances changed as parts were processed sequentially. Now, all sections are processed as a single transaction and this enables Ref Des preservation after Part Manager updates.

Automatic Purging of Bus Bits

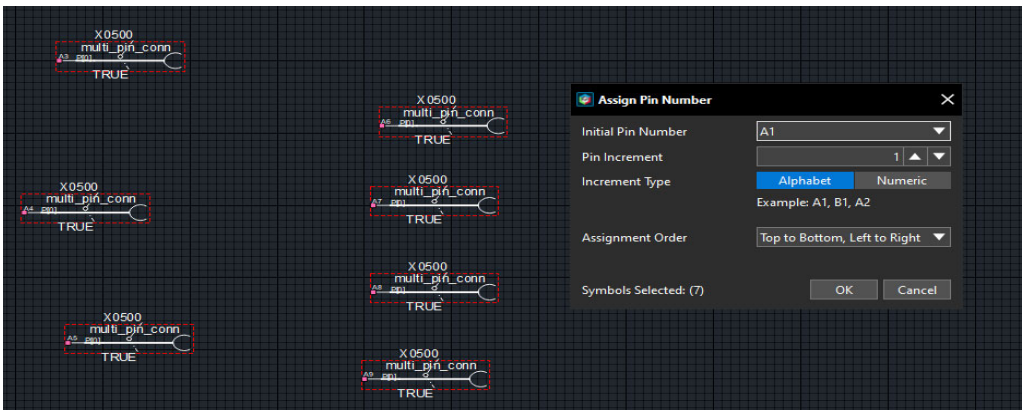
If there was a change in the interface from a hierarchical block and the number of bits was reduced, you had to manually purge the bus bits using the *Tools – Purge Bus Bits* command. Such deleted bus bits are now automatically purged. As a result the *Tools – Purge Bus Bits* command has been withdrawn.

Important

Designs created or updated in any release later than Release 17.4-2019 HotFix 030 are fully backward compatible and can be opened in earlier versions. To avoid any data inconsistency, it is recommended that you do not edit designs in an earlier release. However, if you must make changes in an earlier release, ensure that you use the `runDBDoctor` Tcl command in the correction mode in the latest release.

Connector Pin Assignment

When working with single-pin multi-section components, you can now select a group of components on the schematic canvas and assign pin numbers based on data from the part definition (`chips.prt`).



Variants Flow

You can now replace components in variants with placeholders. Preferred parts are no longer restricted to parts available in the project libraries. In addition, you can mark components on the base design also as DNI.

- Programmable Parts in Variants
- Show Crosses for PACK_IGNORE Components

Programmable Parts in Variants

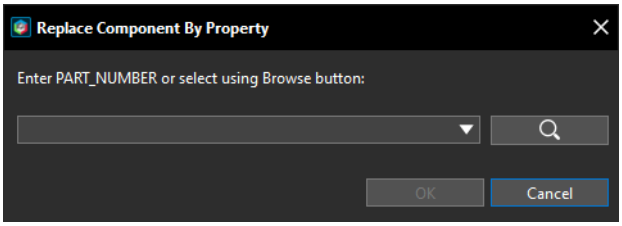
Important

Available only when connected to a Remote Pulse Server.

You can now specify a part code and add a preferred part regardless of the availability of parts in project libraries. To use this feature, the following two directives need to be set in the `START_VARIANT` section of the `site` or *`project`* cpm file:

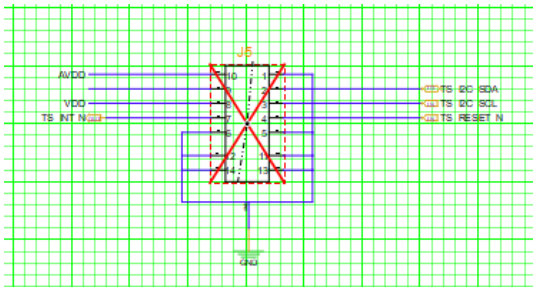
Directive	Value	Description
`VAR_REPLACE_BY_PROP`	`ON`	Enables the feature
`VAR_REPLACE_PROP`	*`<Property name>`*	Specifies which property can be changed for the component. For example: `VAR_REPLACE_PROP 'PART_NUMBER'`

With these directives enables, when you click *Add Preferred Part* for any variant, the following dialog box shows. You can enter a placeholder part number or browse through the available parts and choose one.

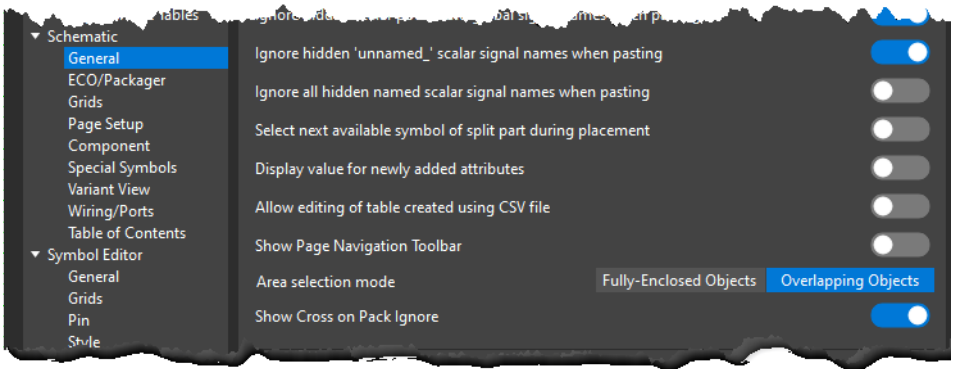


Show Crosses for PACK_IGNORE Components

The visual cue for Do Not Install (DNI) components on variants is now available for the base design too. A cross appears over any component with the `PACK_IGNORE` property set to `TRUE` as shown in the following image:



To enable this feature, select *the Show Cross on Pack Ignore* option in the *Schematic – General* preferences.



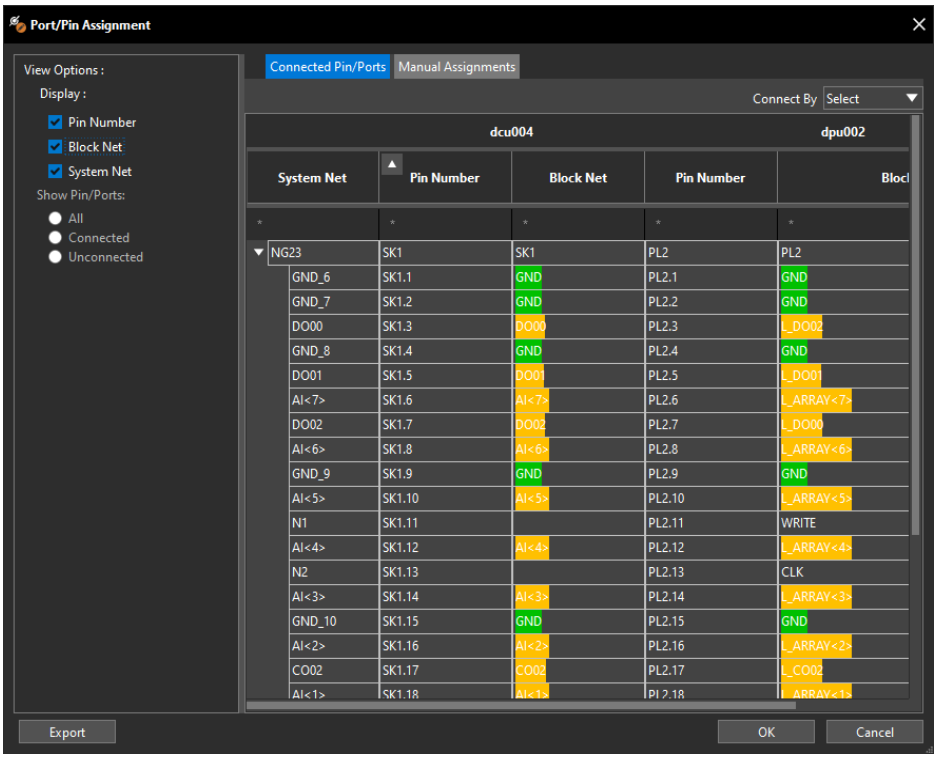
System–Level Design Enhancements

When working with system-level designs, you can now set up color coding in the Port/Pin Assignment dialog box and even print the designs.

- Port/Pin Assignment Colors Coding
- Printing System-Level Designs

Port/Pin Assignment Colors Coding

The *Port/Pin Assignment* dialog box shows the connectivity across block pins. To help quickly identify the nets that are perfect matches or partial matches, you can enable the color coding.



To enable this feature, set the following directives:

Directive	Value	Description
`PIN_ASSIGNMENT_DIALOG_SHOW_COLORED_NET_MISMATCH`	`Yes`	Enables the feature

Directive	Value	Description
PIN_ASSIGNMENT_DIALOG_MINIMUM_CHARACTER_MATCH_COUNT	*<number>*	The number of characters that should match, such as 3.

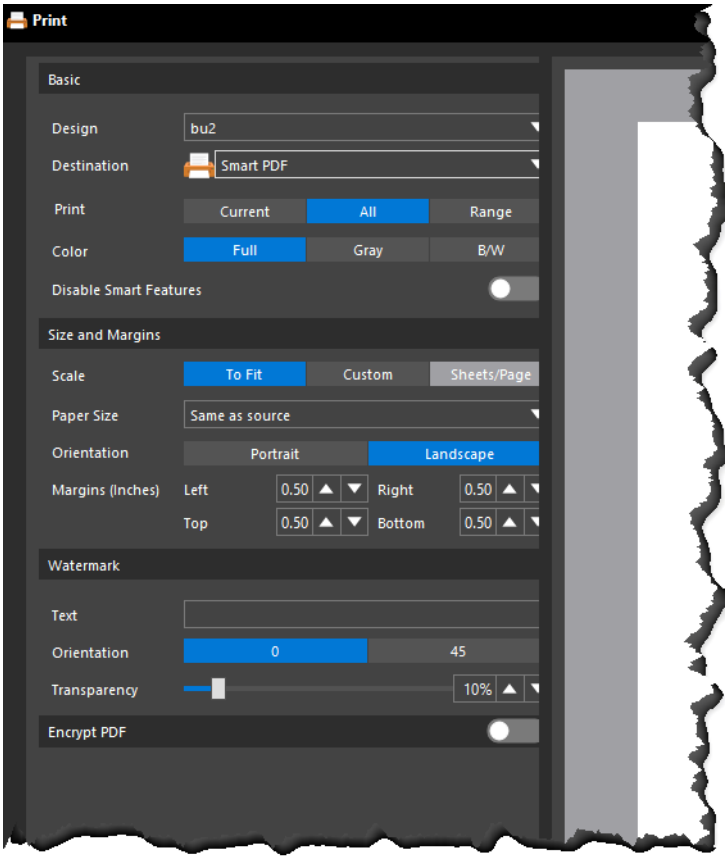
Here is how the colors are assigned:

- If all characters match, the net is highlighted in green
- If ‘N or more’ continuous characters match but not all, the net is highlighted in yellow.
- If less than ‘N’ characters match, the net is highlighted in red.

You can also set custom colors for reporting the net name mismatches using a Tcl script.

Printing System-Level Designs

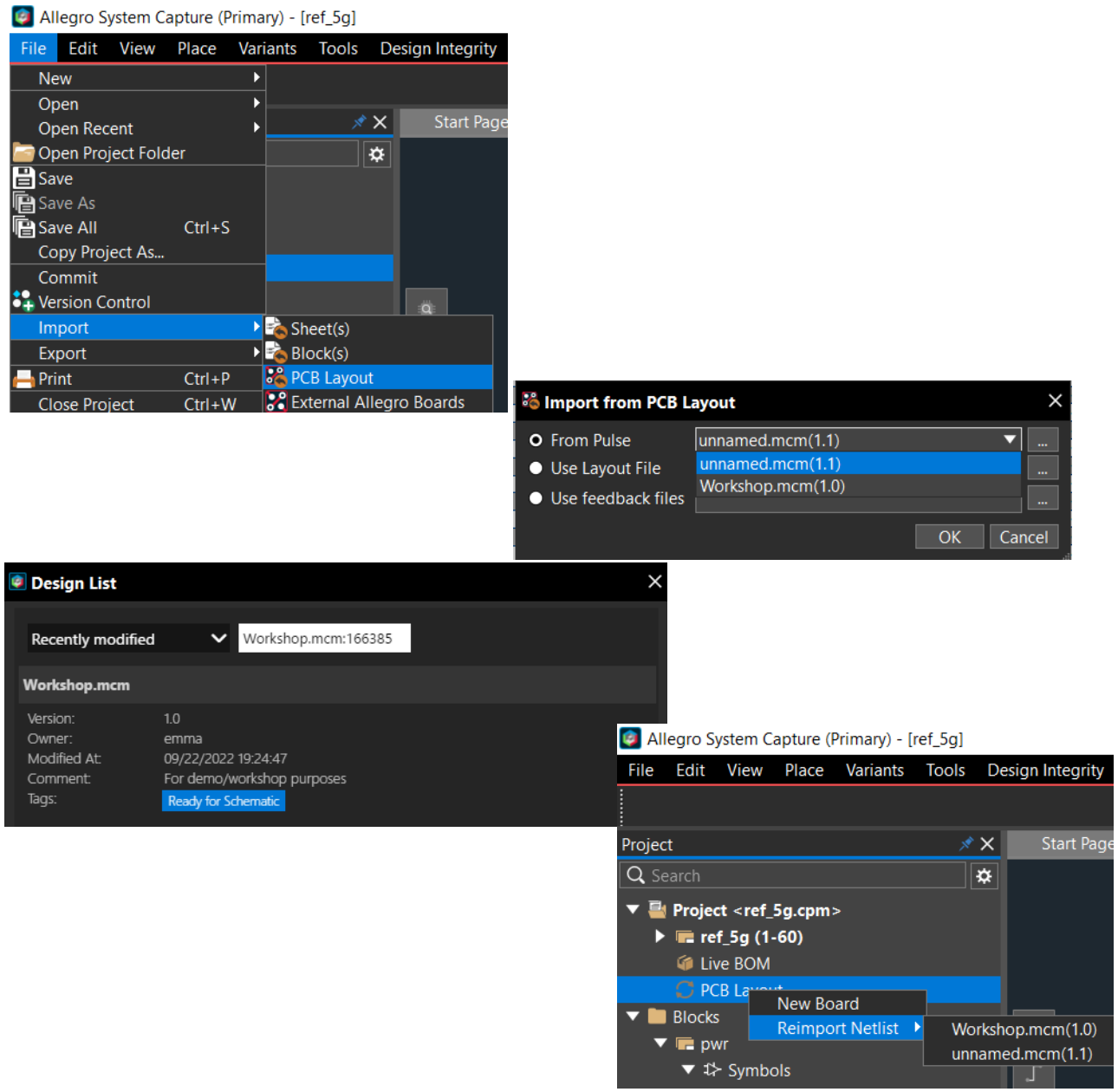
You can now print system-level designs to all print formats, such as print, PDF, Smart PDF, and so on, just as schematic designs. Blocks are printed in the top-down order, without any repetition.



Importing .MCM Files Supported

In Pulse, you can maintain a link between the schematic design version which was used to generate the netlist for the layout, and the layout version that was backannotated to the schematic. This ensures that the schematic and layout design versions are always in-sync.

From this release, in addition to `.brd` files from PCB Editor, you can now also link `.MCM` files from APD Plus and Allegro System Capture schematics.



For details on linking schematics and PCB layouts, refer to *Linking Schematic and Layout Versions* in *Allegro System Capture Pulse User Guide*.

Library Authoring Enhancements

The following enhancements are made in the library authoring solution. These enhancements are available depending on the library format being used:

- In-place Editing Support for Allegro DE-HDL Libraries
- OrCAD Library Editing Enabled

Note: DE-HDL and OrCAD library editing is enabled in the following licenses:

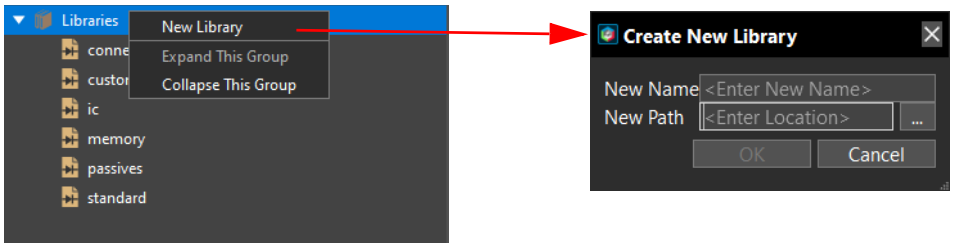
- Allegro System Capture Designer (ASC200)
- Allegro System Capture Venture (ASC300)
- Allegro Managed Library Authoring (PLA300)
- Allegro X EE (ALGX100)
- Allegro PCB Librarian / Allegro Library Authoring (PX3500)

In-place Editing Support for Allegro DE-HDL Libraries

In addition to creating Allegro Unified libraries and parts within System Capture, you can now create DE-HDL libraries and even edit parts within System Capture when working in a DE-HDL libraries project.

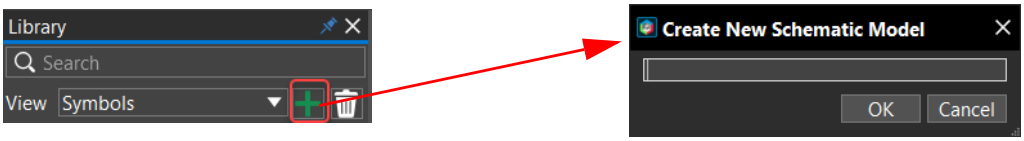
- Creating a new DE-HDL library from the *Project Explorer*

  Right-click *Libraries* and choose *New Library* to start creating a library.

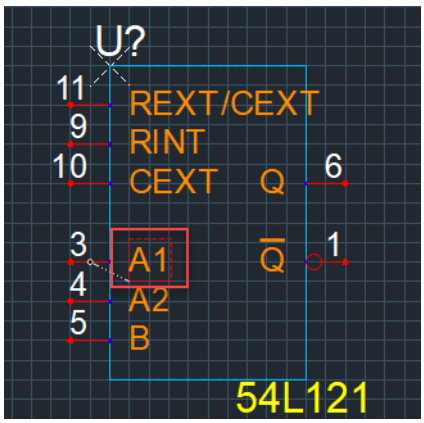


- Creating DE-HDL schematic model

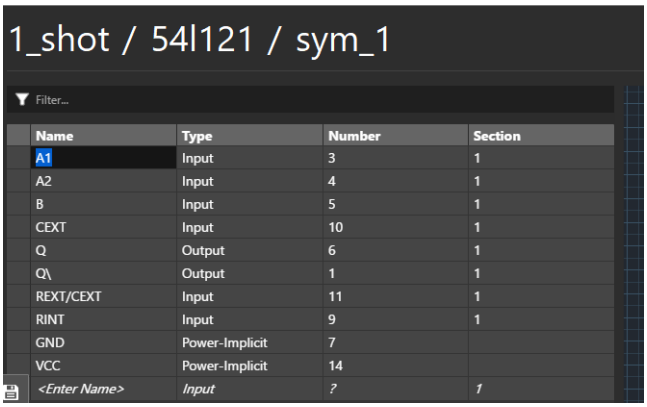
To add a new schematic model, click the *New Symbol* icon and create a new schematic model.



You can edit a library cell in the table view or directly on the canvas.



Editing Cells on Canvas



Editing Cells in Table View

- To view a list of cells in a library, double-click the library.

  Based on the file system permissions, you can create, read, update, or delete the cells.

Important

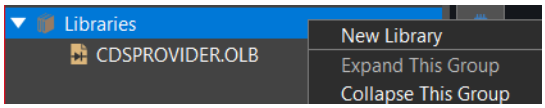
Editing is not supported for sizable parts, multi-primitive parts, tech independent parts, and library-level blocks. To edit these, choose *Tools – Part Developer*.

OrCAD Library Editing Enabled

You can launch OrCAD Capture from System Capture to create a new or edit an OLB schematic model.

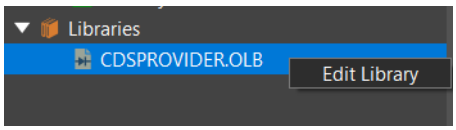
- Adding a new OrCAD library

  Right-click *Libraries* in *Project Explorer* and choose *New Library*.



- Editing an existing OrCAD library

  Right-click a library in *Project Explorer* and choose *Edit Library*.



  OrCAD Capture is launched where you can create or edit the library.

New Audit Rules in Design Integrity

To facilitate and improve design creation and quality, the following audit rules have been added:

Category	Rule Name	Rule Description
Connectivity Checks	Clock pins of ICs not connected to same set of ICs or connectors as MISO and MOSI pins	Reports Clock pins of ICs that are not connected to same set of ICs or connectors as Master Input Slave Output (MISO) and Master Output Slave Input (MOSI) pins.
	MISO and MOSI pins of ICs incorrectly connected to non-MISO or non-MOSI pins	Reports MISO and MOSI pins of ICs that are incorrectly connected to non-MISO or non-MOSI pins
	MISO and MOSI pins of ICs not connected to the same set of ICs or connectors	Reports MISO and MOSI pins of ICs that are not connected to the same set of ICs or connectors
	Nets not connected to off-page port	Reports nets that are present on multiple pages but are not connected to an off-page port Instead of highlighting violations of this rule instance by instance, Schematic Audit highlights the pages where the violation occurs making it easier to correct it.
	Unconnected Chip Select pins of ICs when MISO or MOSI pins are connected	Reports Chip Select pins of ICs that are not connected when MISO and MOSI pins are connected
	Unconnected Clock pins of ICs when MISO or MOSI pins are connected	Reports Clock pins of ICs that are unconnected when MISO and MOSI pins are connected
	Unconnected MISO and MOSI pins of ICs	Reports MISO and MOSI pins of an IC when either MISO or MOSI pin of an IC is connected, but not both

Category	Rule Name	Rule Description
Graphical Checks	Invalid net name	Reports if a net name has invalid characters in it
	RefDes visibility	Reports the invisible reference designators for components for a specified reference designator pattern
Mechanical Checks	Fiducials not present	Reports if fiducials are not present in the design
	Fiducials present is less than the minimum specified limit	Reports if the number of fiducials present is less than the minimum specified limit
	Holes not present	Reports if holes are not present
	Testpads not connected to a net having user-defined name	Reports if testpads are not connected to a net having user-defined name
	Testpads not present	Reports if testpads are not present
Power Net Checks	Low-voltage class net having incorrect voltage	Reports nets of low-voltage class having voltage greater than the threshold voltage
	Nets connected through discretes belonging to different net classes	Reports nets connected through discretes R,L,C that belong to different net classes
	Voltage net missing net class	Reports nets with voltages missing net class

Customization using Tcl and Directives

This section lists the:

- Updated Tcl Commands
- New Directives Added

Updated Tcl Commands

The following commands have been added or modified in this release:

- `setMonochromePrintingThreshold`
- `setDockWidgetFloating`
- `registerCommand`
- `setCloseTCLHandler`
- `openHybridDock`
- `setDockWidgetUndockDefaultSize`
- `dbGetDesignPages`

See the *Tcl Commands Reference Guide* for details.

New Directives Added

The following directives have been added in this release:

- `ALLOW_HFS_SWAPS`
- `BASE_NET_OVERLAY`
- `delete_folders_on_copyproj`
- `EXPLICIT_BASE_NET_IDENTIFIER`
- `IGNORE_HIDDEN_SCALAR_POWER_SIGNAL_NAMES_WHEN_PASTING`
- `IGNORE_HIDDEN_SCALAR_SIGNAL_NAMES_WHEN_PASTING`
- `IGNORE_HIDDEN_UNNAMED_SCALAR_SIGNAL_NAMES_WHEN_PASTING`
- `IMAGE_COLOR_MODE_PRINT`

- MONOCHROME_PRINTING_THRESHOLD
- PIN_ASSIGNMENT_DIALOG_SHOW_COLORED_NET_MISMATCH
- PIN_ASSIGNMENT_DIALOG_MINIMUM_CHARACTER_MATCH_COUNT
- rename_folders_on_copyproj
- SHOW_ALL_BLOCKS_FOR_IMPORT
- SHOW_POWER_SIGNAL_NAMES_FOR_NEW_CONNECTIONS
- VAR_REPLACE_BY_PROP
- VAR_REPLACE_PROP

See the *Allegro Front-End CPM Directive Reference Guide* for details.

OrCAD Capture CIS

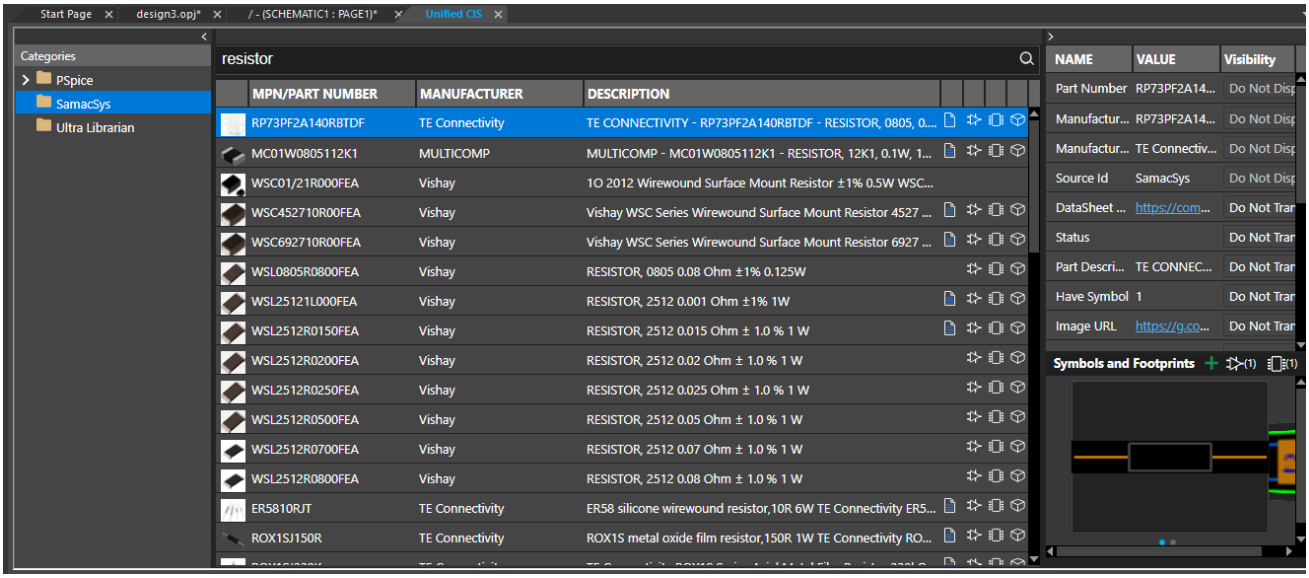
This section describes the following enhancements and new features in OrCAD® Capture CIS in release 22.1.

Unified Component Information System (CIS)

Unified CIS is a component management system that provides an intuitive user interface to access components from various sources, without any additional overhead of creating a preferred part database and setting up an ODBC data source.

From the Unified CIS interface, you can view, search, and place components in an OrCAD Capture design from the following sources:

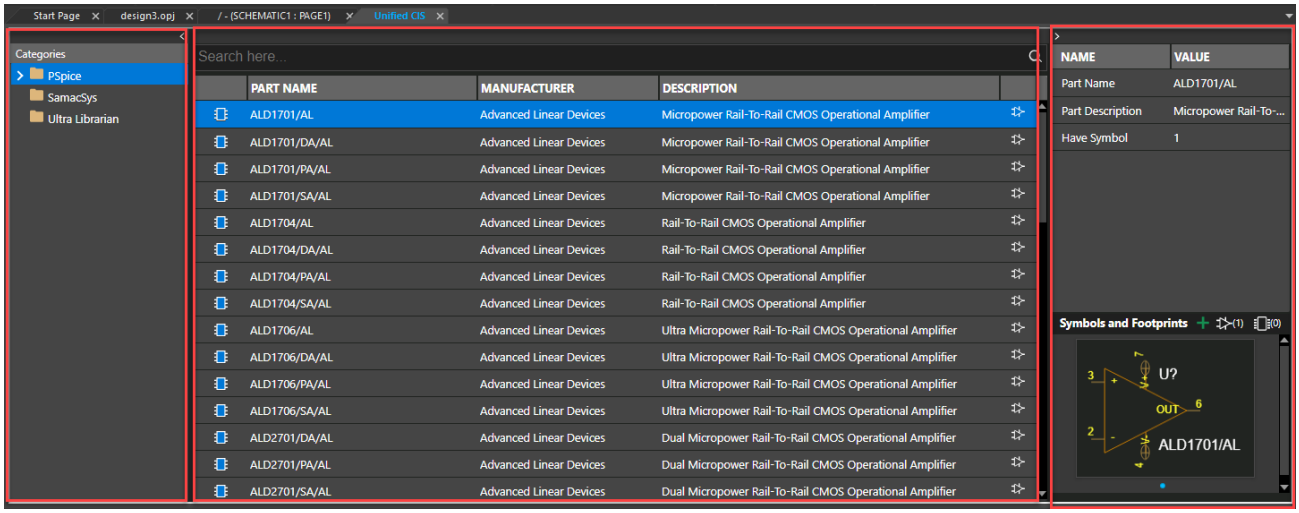
- Cadence-supplied PSpice libraries
- Cadence-supported external content providers – SamacSys and Ultra Librarian



Access the following functions from the Unified CIS interface:

- View components and their properties
- View symbols and footprints
- Place components on schematic

Select a source from the *Categories* browser (left pane). View details of components from different sources in the enhanced part browser (middle pane). View property details of components in the properties browser (right pane).



For detailed information on Unified CIS, refer to *OrCAD CIS User Guide*.

PSpice and PSpice Advanced Analysis

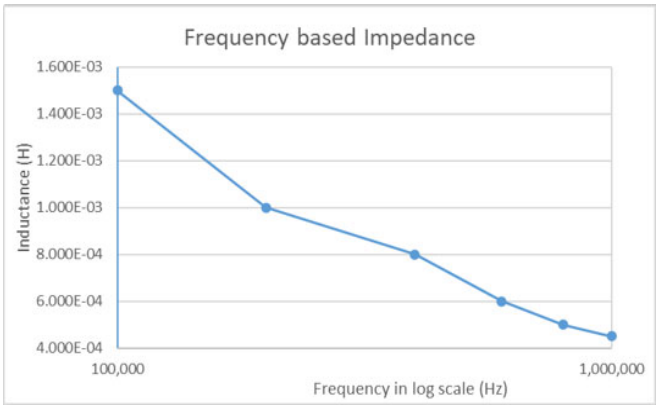
This section describes the following enhancements and new features in PSpice® and PSpice® Advanced Analysis in release 22.1.

Creating Frequency-Based Impedances Using Behavioral Sources

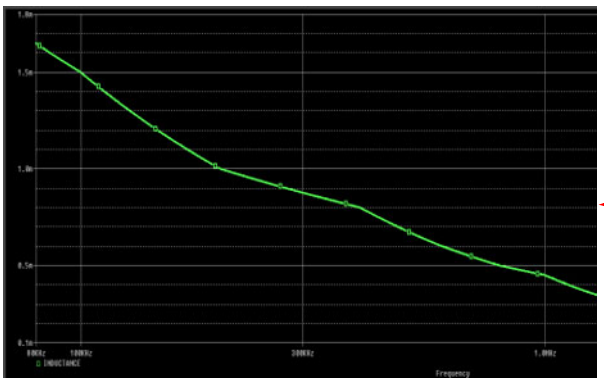
Release 22.1 provides a convenient way to implement an impedance that varies with frequency, using frequency tables in the CSV format. To support this feature, two new components, `GFREQ_FILE` and `EFREQ_FILE`, are added to the Cadence library, `abm.olb`, which is available from the following location:

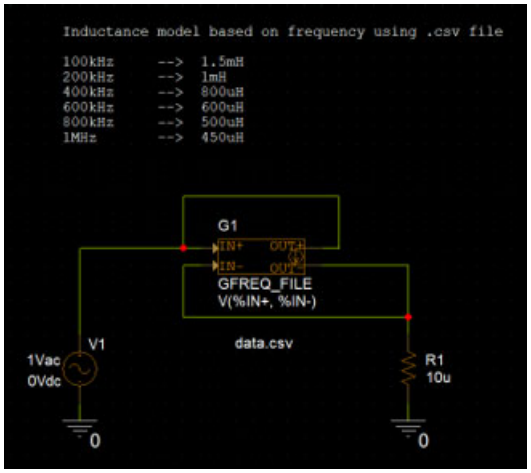
`<install_dir>/tools/capture/library/pspice/abm.olb`

In the frequency table, you can specify values for [`Frequency`, `Real`, and `Imaginary`], or [`Frequency`, `Magnitude`, and `Phase`] as shown in the following set of images:

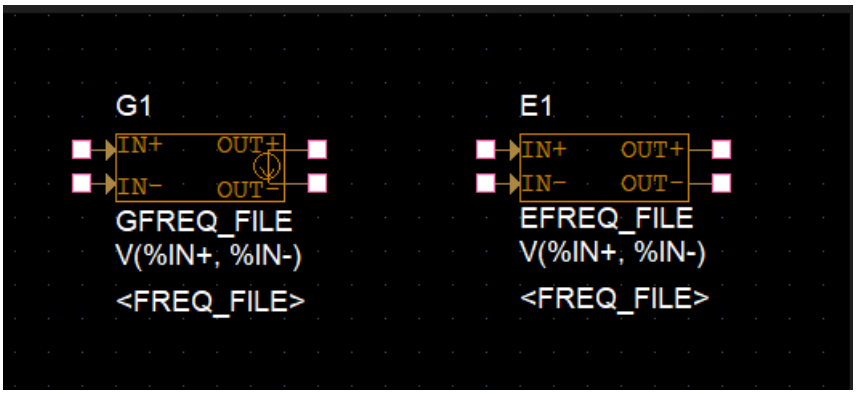


	A	B	C
1	10k	0.00397887	90
2	100k	0.00106103	90
3	200k	0.00079577	90
4	400k	0.00049736	90
5	600k	0.00044210	90
6	800k	0.00039789	90
7	1meg	0.00035368	90
8			

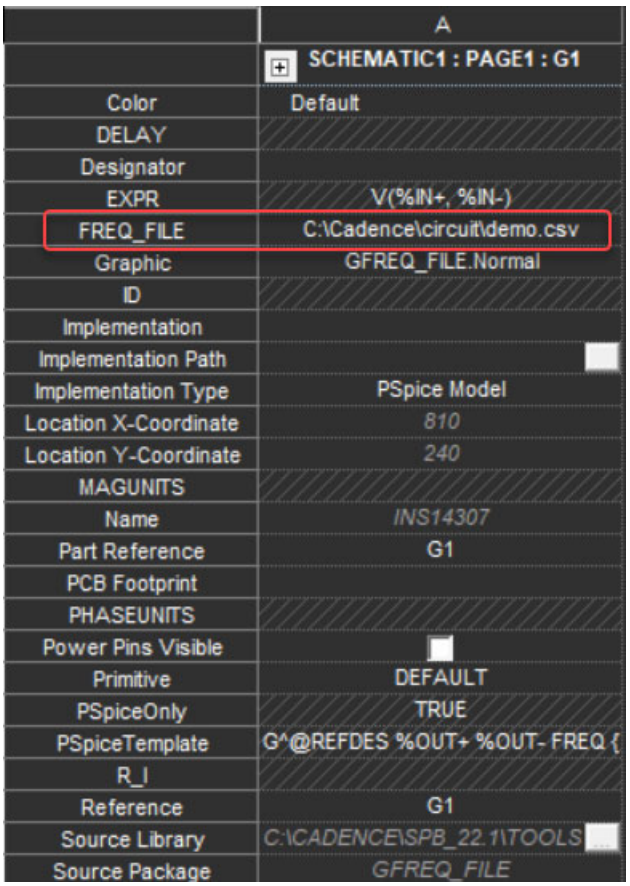




To use the components in the design, place either `GREQ_FILE` or `EFREQ_FILE` from `abm.olb` on the canvas.

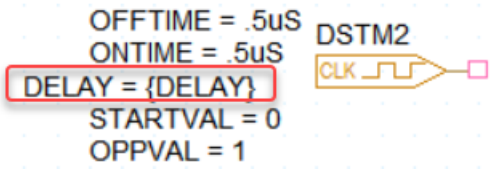


You can then open Property Editor for one of the placed components, and specify the path to the CSV file in the value field of the `FREQ_FILE` property as shown in the following image:



Expression Support for Digital Clock Source

The support for expressions in PSpice® Modeling Application has now been extended to digital clock source, *DigClock*.



Noise Analysis Output Enhancements

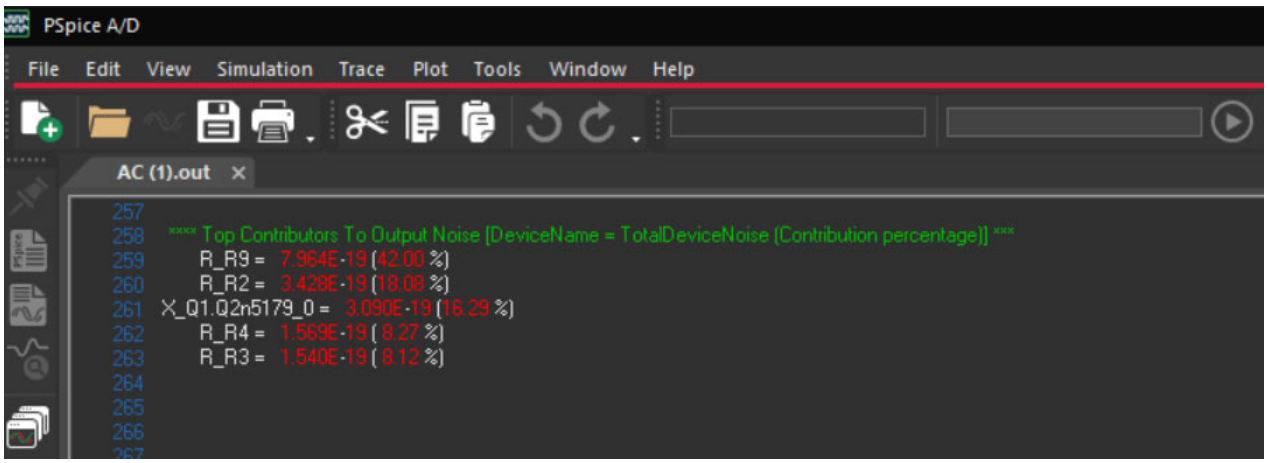
Now, you can set the number of top noise contributors to be reported for Noise Analysis using the `PRINT_NOISE_DISTRIBUTION` option.

For example, to report the top seven noise contributors, use the following syntax:

```
.OPTIONS PRINT_NOISE_DISTRIBUTION =7
```

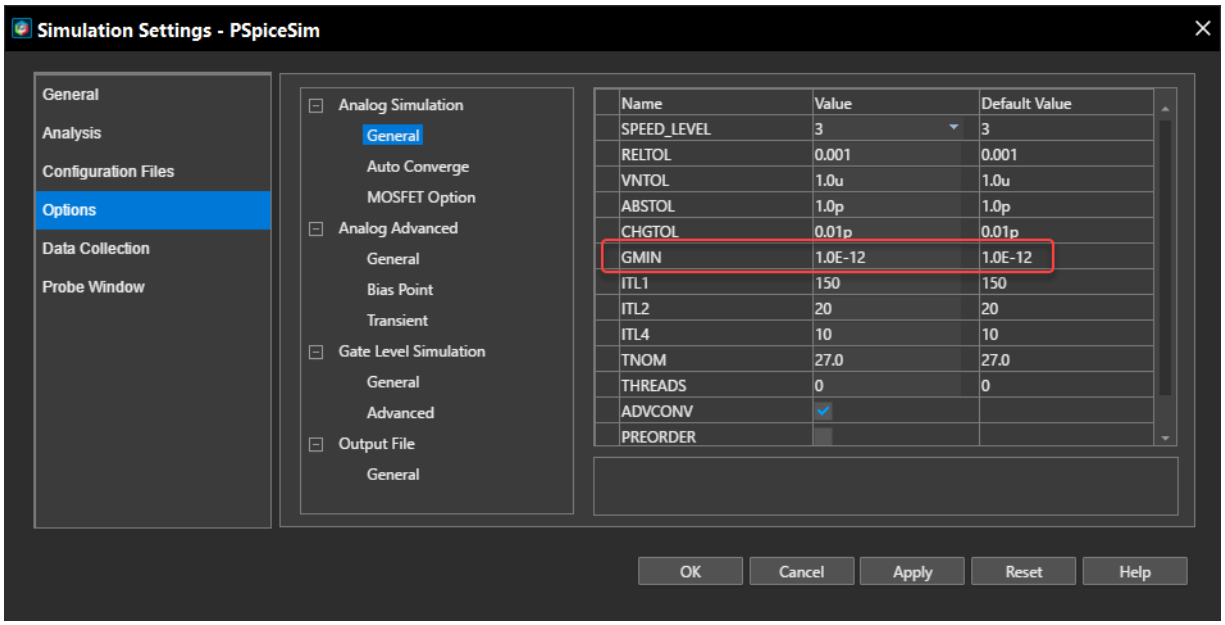
By default, only the top five noise contributors are reported.

If the number of devices is less than the number of top noise contributors, the noise contribution of all the devices is printed.



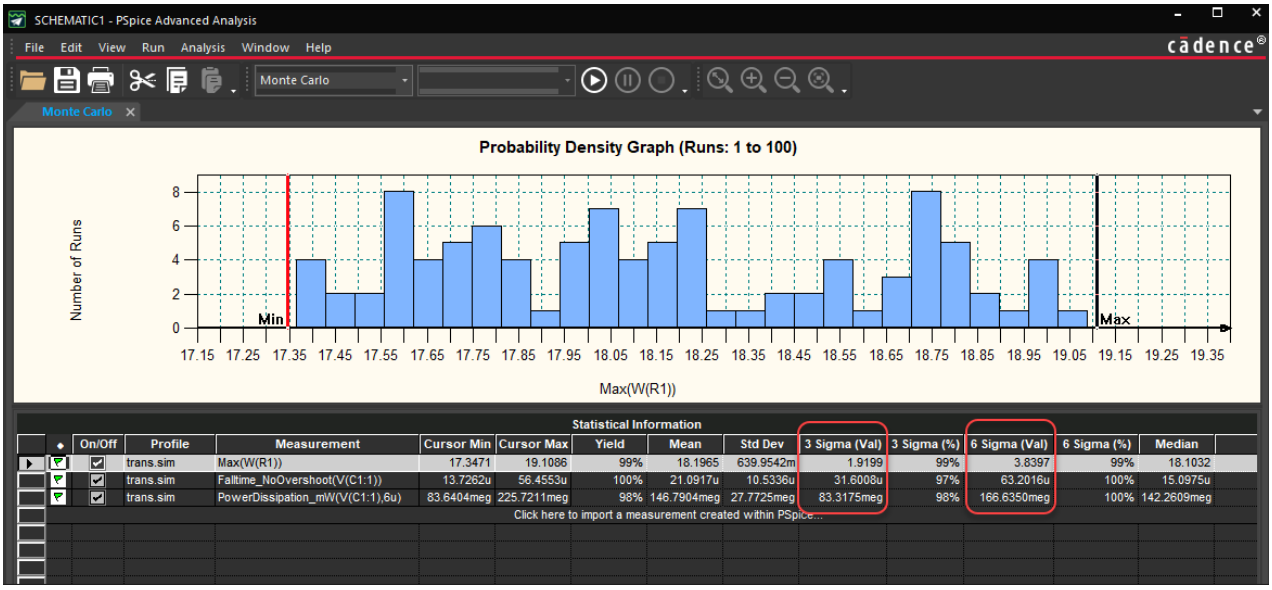
Enhancement for Zero Value Resistors

Circuits can now be simulated with zero value resistors. All the zero values are replaced by `GMIN`, which is set to `1.0E-12` by default. You can edit the value of `GMIN`, if required.



Calculating 3-Sigma and 6-Sigma Values in Monte Carlo Analysis

The Monte Carlo analysis is enhanced to calculate and report 3-Sigma and 6-Sigma values. The sigma values are shown as columns in the Monte Carlo statistical results grid.

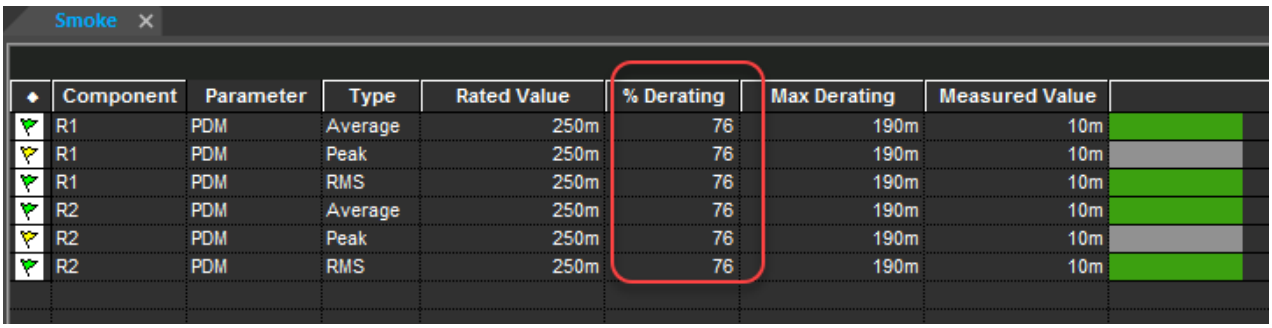


Enhancements in Smoke Analysis

With Smoke analysis, you can enable automatic deration of power and filtering of hierarchical components in Smoke results.

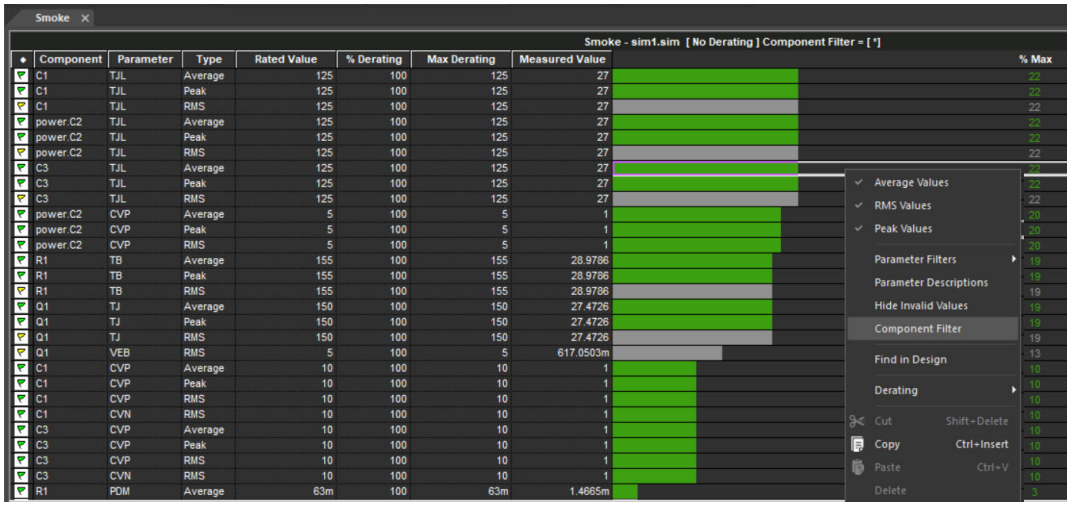
- If custom deration is defined for a resistor, its power dissipation is derated with temperature. The calculated derating value is displayed in the Smoke results window.

.

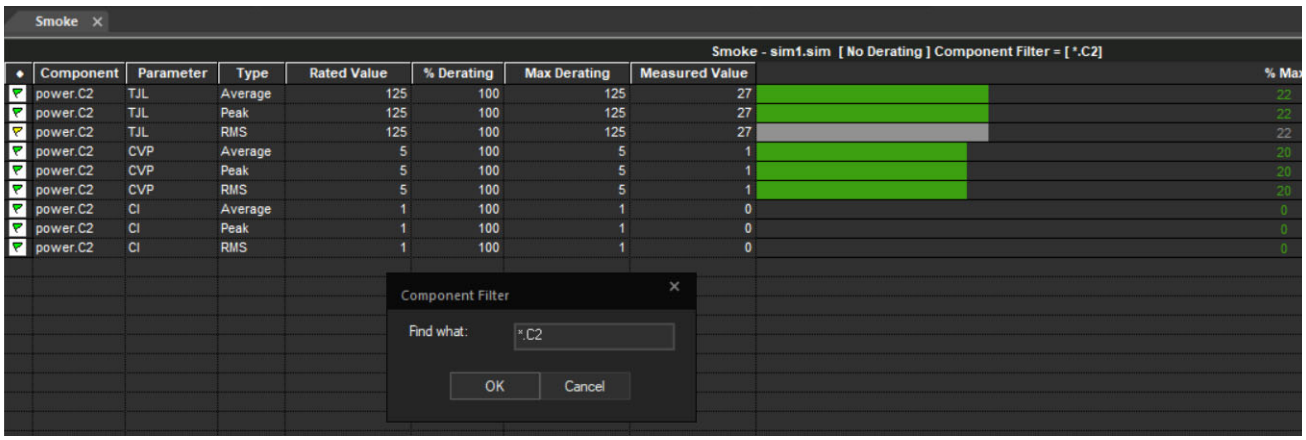


- Hierarchical components can now be filtered by using an asterisk to match any pattern following or preceding a string. To search for components, use the *Component Filter* shortcut command.

  For example, to display all the resistors from the `POWER` block, right-click the component and choose *Component Filter* in the Smoke Analysis window. You can then specify `*.C2` or `*Power.C2` to match all the capacitors in the `POWER` block.



  The filtered components are displayed in the Smoke Analysis window.

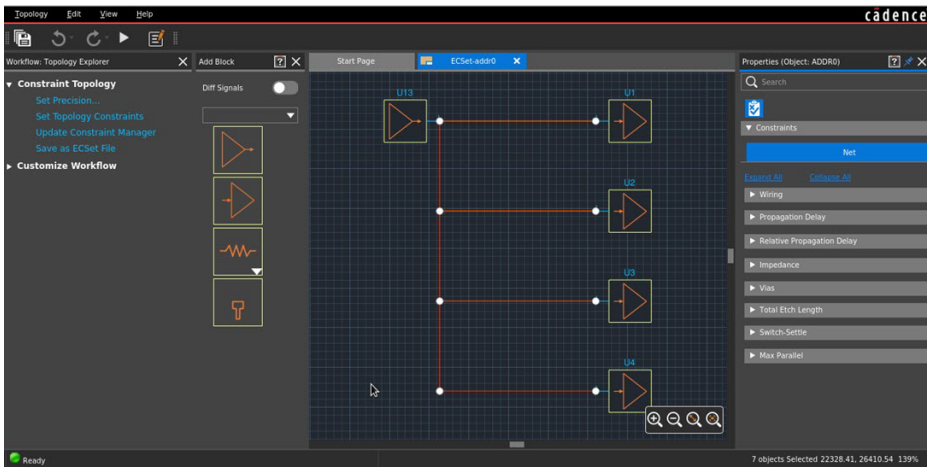


Sigrity Aurora

This section describes the following enhancements and new features in Sigrity™ Aurora in release 22.1.

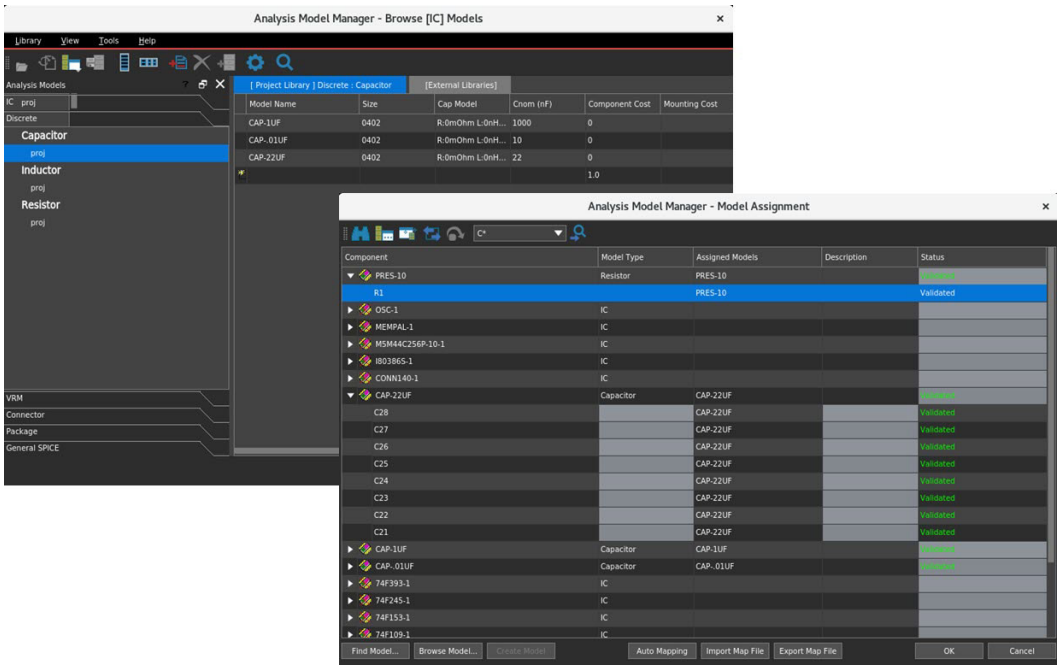
Topology Editor in Allegro PCB Editor and Allegro Package Designer Plus

A *non-analysis* version of Topology Workbench for constraint capture is now included with Allegro® PCB Editor and Allegro® Package Designer Plus.



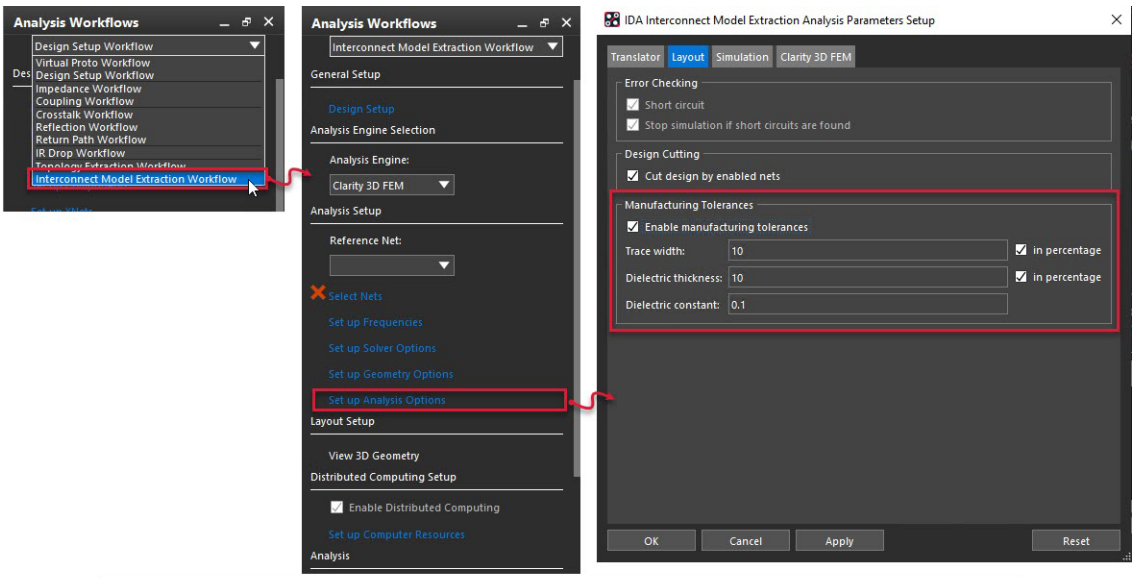
Analysis Model Manager Update

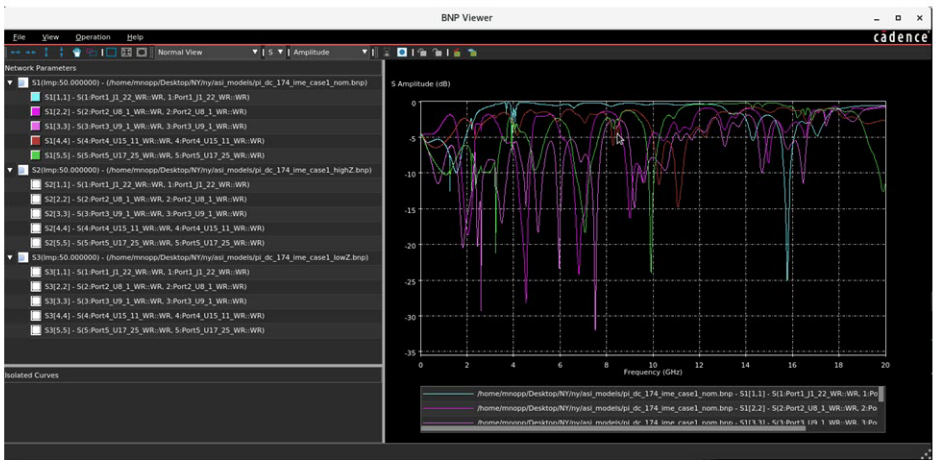
The latest Analysis Model Manager module is integrated with Sigrity™ Aurora similar to the other Sigrity applications and workflows.



Manufacturing Tolerances Definition for Interconnect Model Extraction

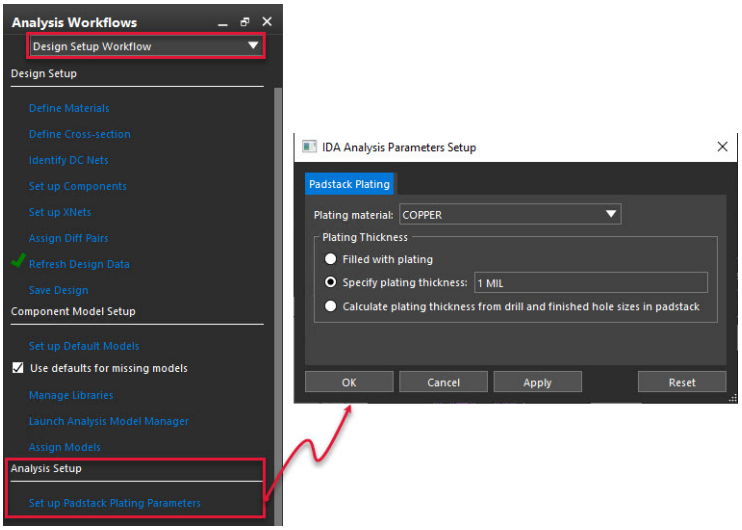
In the *Interconnect Model Extraction Workflow*, you can define manufacturing tolerances around layout database. This automates the extraction of high and low impedance scenarios along with the *as-designed* case.





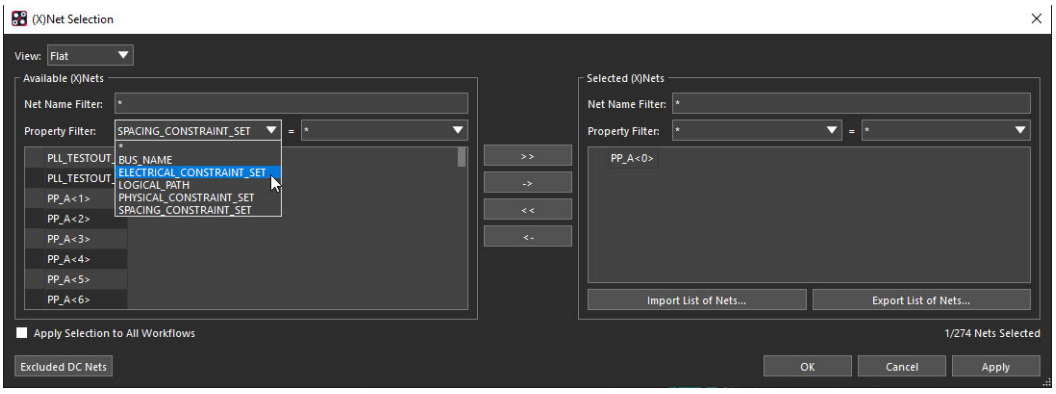
Via Plating Thickness Control Added

In the *Design Setup Workflow*, the *Set up Padstack Plating Parameters* option is added to globally define the via plating thickness for Sigrity™ Aurora.



Net Selection by List

An ease-of-use improvement is incorporated in the Net Selection form to generate and load lists of nets to select for analysis.



Topology Workbench

This section describes the following enhancements and new features in Topology Workbench in release 22.1.

Common Update: Renamed TopXp.exe to TopWb.exe

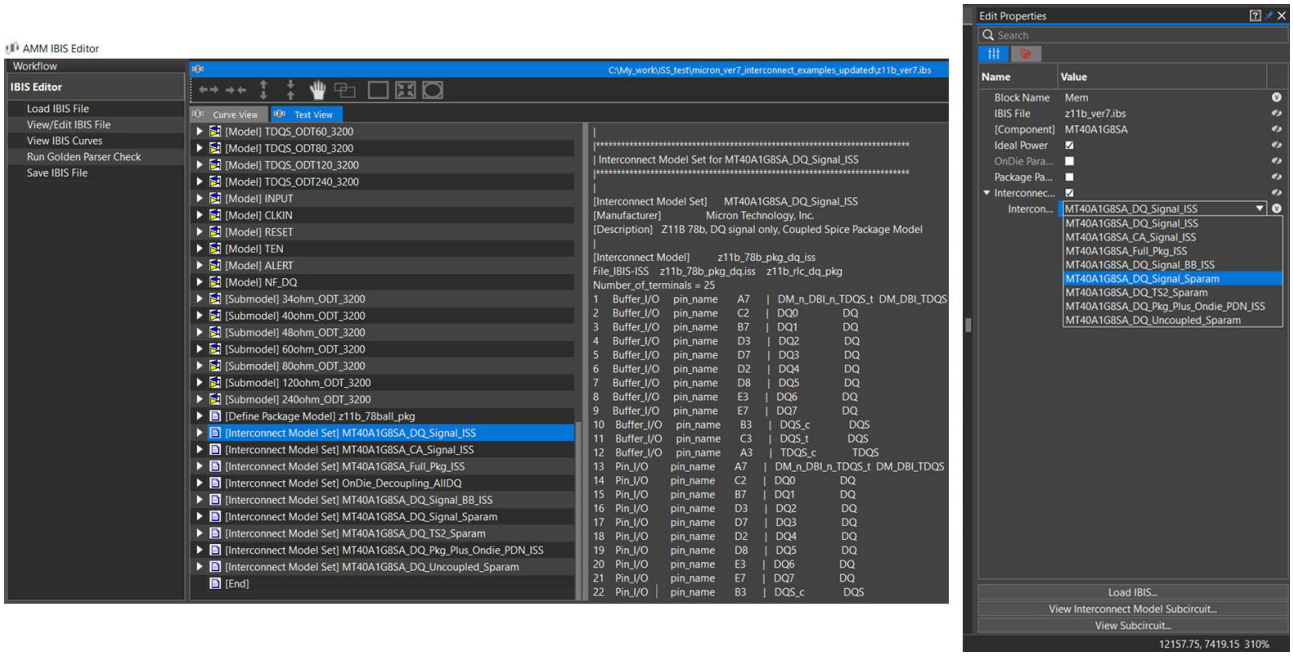
A common update to the release is the renaming of the Topology Workbench executable file from `TopXp.exe` to `TopWb.exe`.

SystemSI Updates

- IBIS ISS Package Model Supported
- Trace Editor GUI Changes
- Availability of Coaxial Cable Modeler
- PCI Express Gen 6 Compliance Kit Supported

IBIS ISS Package Model Supported

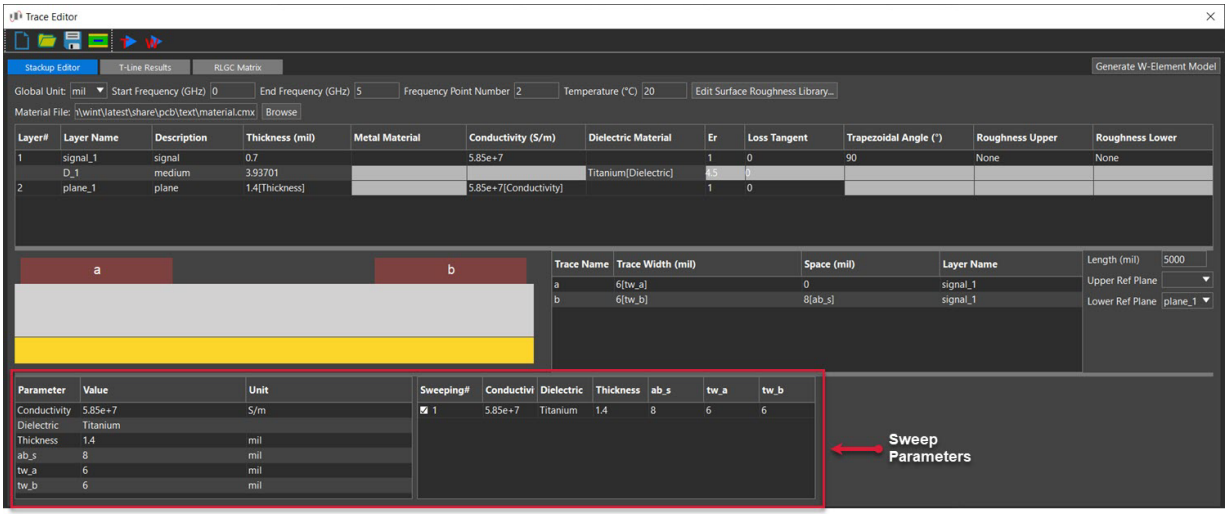
The SystemSI workflows are now compliant with IBIS 7.1 specifications to enable modeling of complex packages.



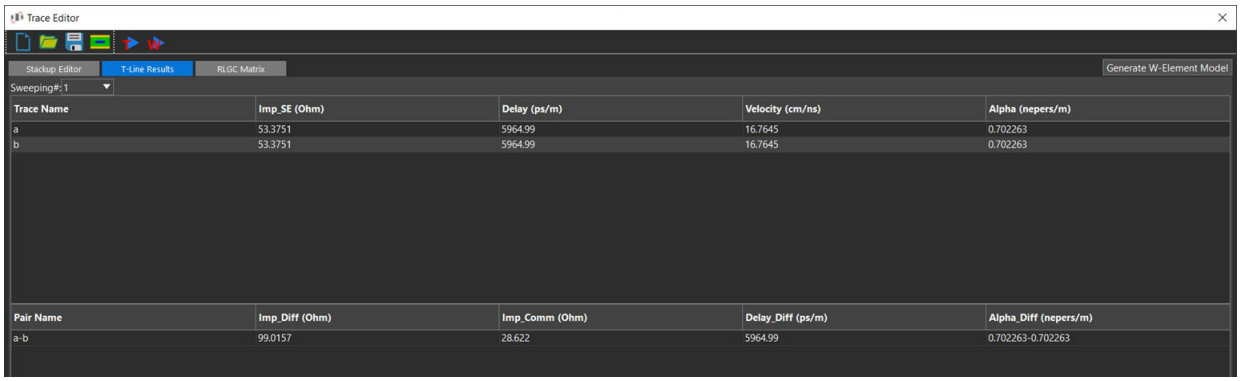
Trace Editor GUI Changes

The Trace Editor interface is enhanced to include the following changes:

- You can now set up sweep parameters as well in Trace Editor.



- The tables generated based on the sweep parameters are enhanced too.

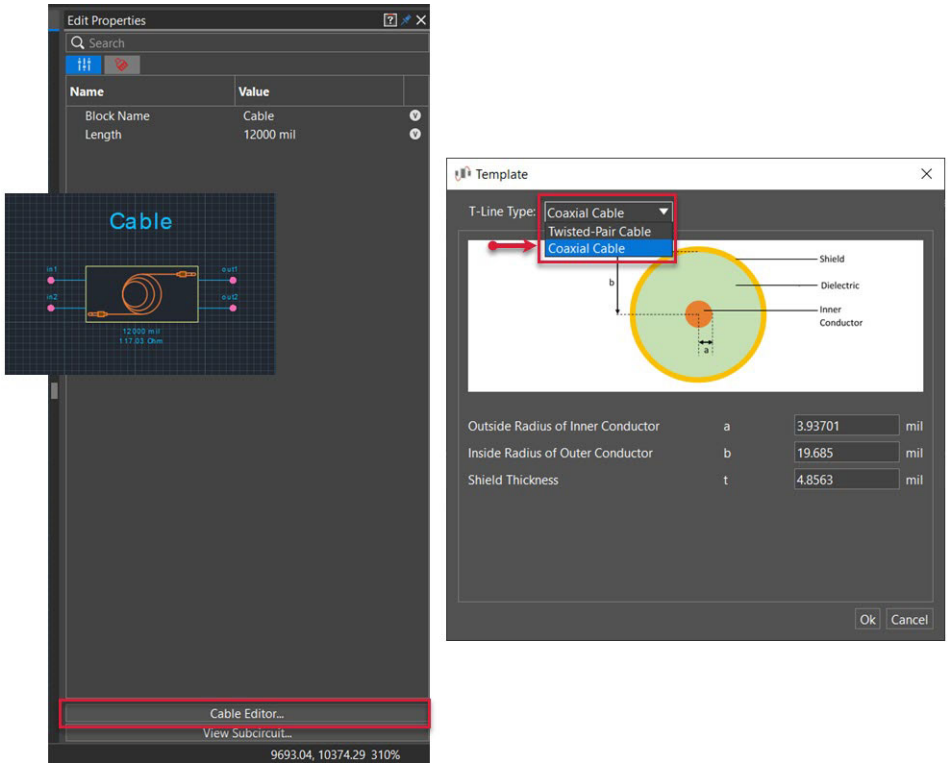


Availability of Coaxial Cable Modeler

For a Cable modeler block, you can now choose to define parameters for a coaxial cable.

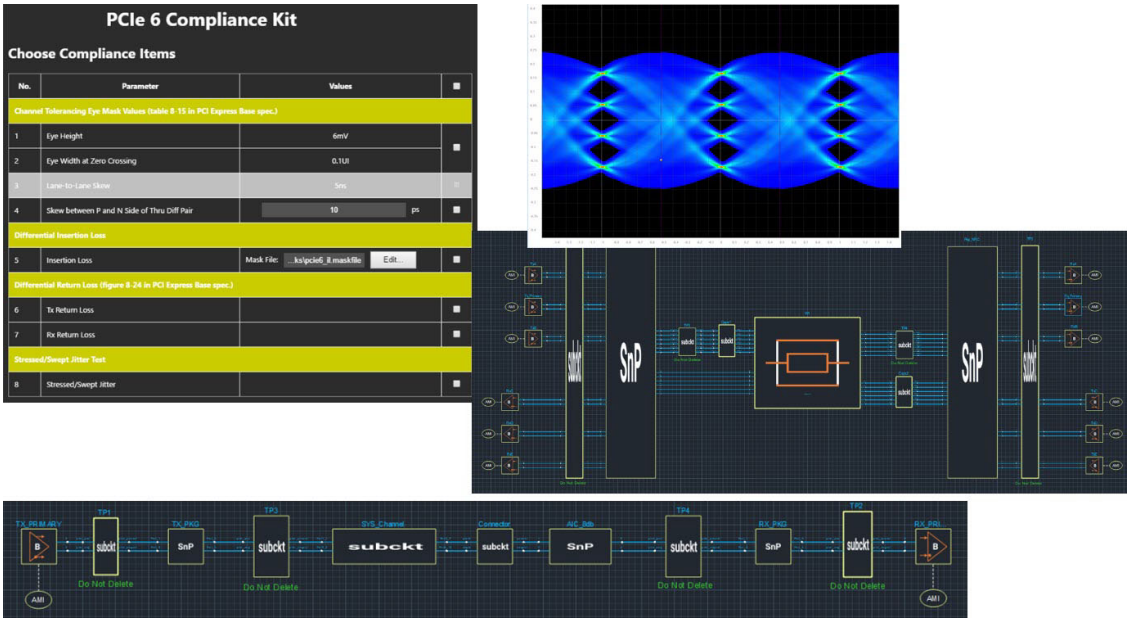
The choice between Twister-Pair Cable and Coaxial Cable can be made from the T-Line Type list displayed in the Template form. To access this form, open the Cable Editor from the Edit

Properties panel of the Cable modeler block and then click *Input From Template* in the editor's menu.



PCI Express Gen 6 Compliance Kit Supported

To support the first mainstream usage of PAM4 signaling, the SystemSI workflows in Topology Workbench let you select and simulate PCI Express Gen 6 Compliance Kit items.



SystemPI Updates

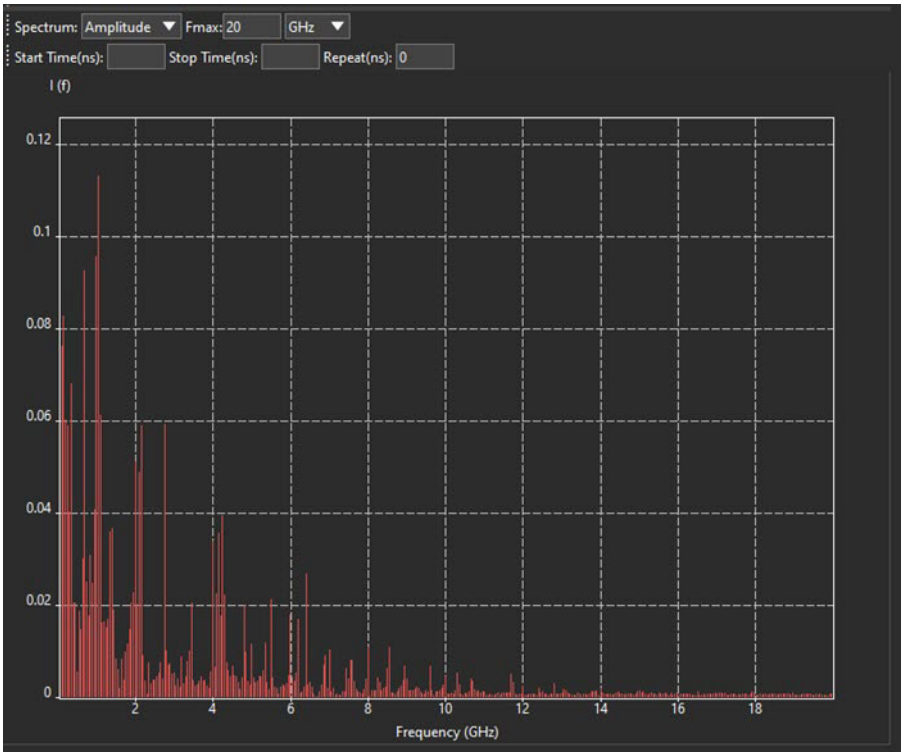
- Editing of Voltus Model PWLs Supported
- Frequency Spectrum Enhancements

Editing of Voltus Model PWLs Supported

The modified Voltus files are now saved in the `asi_models` directory.

Frequency Spectrum Enhancements

You can now select the start and stop window of a waveform. In addition, the frequency spectrum can be periodic or non-periodic.



Documentation Update

In this release, Topology Workbench Tcl Command Reference is added to the documentation set. This manual covers information about the Tcl commands supported in Topology Workbench. These Tcl commands can be used internally when designers perform tasks using the interface menu options of Topology Workbench. Anyone who needs to create scripts to modify the default built-in functionality, or wants to accomplish design tasks without clicking and navigating the user interface can also use these Tcl commands.